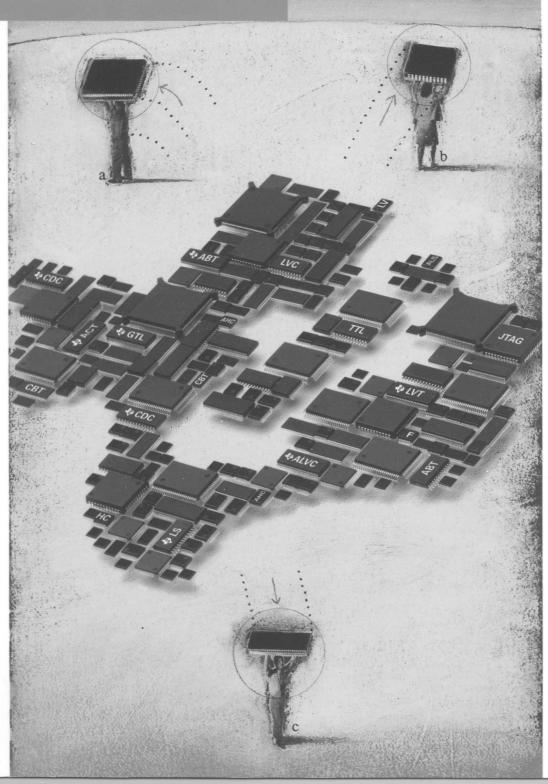


Logic Selection Guide Second Quarter 1997



LOGIC OVERVIEW	1	CONTRACTOR CONTRACTOR CONTRACTOR
FUNCTIONAL INDEX	2	THE PERSON NAMED IN COLUMN
FUNCTIONAL CROSS-REFERENCE	3	
DEVICE SELECTION GUIDE	4	

IMPORTANT NOTICE

LOGIC SELECTION GUIDE

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Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Orthoal Applications").

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CONTACTS/INFORMATION

Advanced System Logic (ASL) Advanced Bus Interface (ABI)

PRODUCT INFORMATION CENTER

(972) 644-5580

LITERATURE REQUESTS

(800) 477-8924

TI HOME PAGE

http://www.tl.com

TI ASL HOME PAGE

http://www.tl.com/ sc/docs/asl/home.htm

TI DATA SHEETS

http://www.tl.com/ sc/docs/psheets/plds.htm

TEXAS INSTRUMENTS

P.O. Box 84, M/S 835 Sherman, TX 75091 USA Fax: (903) 868-5980 Texas Instruments (TI) offers a full spectrum of logic functions in a variety of technologies. TI's process technologies include CMOS, bipolar, and BiCMOS. These state-of-the-art process technologies offer the logic performance and features required in today's system designs. TI's product offerings include the following:

- · ABT, ABTE, AC, ACT, AHC, AHCT, ALB, ALS, ALVC, AS
- BCT, BTA, CBT, F, FB, FIFO, GTL, HC, HCT
- JTAG, LS, LV, LVC, LVT, S, SSTL, TTL

TI has addressed many important design issues, including testability, memory driving, bus termination, low skew requirements, and low-impedance line driving with specialized, advanced logic devices that improve overall system performance.

TI offers a wide variety of packaging options, including advanced packaging such as the plastic thin quad flat package (TQFP), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin very small-outline package (TVSOP). All of these deliver high performance and allow the designer to double input/output in the same board area or to reduce the board-area requirement by half.

For further information on logic families, refer to the list of current Advanced Logic publications provided in this preface. For an overview of Tl's logic families, see Section 1. This selection guide lists the functions that Tl offers in each logic family, along with the current schedule and applicable literature number. The literature number identifies the current data sheet, which can be ordered through your local sales office or Tl authorized distributor (refer to the back cover of this guide). Many Tl data sheets are available on the World-Wide Web at http://www.ti.com.

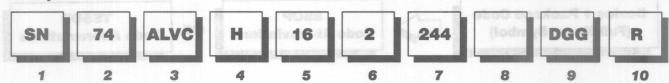
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TI ADVANCED LOGIC PUBLICATIONS

Listed below is the current collection of TI logic technical documentation. These documents can be ordered through a TI representative or authorized distributor by referencing the literature number.

technologies. The propess techn TRAMUDOO de CMOS, bipolist, and Bi Thesa state of the sat process technologies offer the logic performan	LITERATURE NUMBER
AC/ACT CMOS Logic Data Book (1997)	SCAD001D
AC/ACT Logic Product Information (1996)	SCAA027
Advanced BiCMOS Technology Data Book (1994)	SCBD002B
Advanced Bus-Interface SPICE I/O Models Data Book (1995)	
Advanced CMOS Logic Data Book (1993)	SCAD001C
AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book (1996)	SCLD004
ALS/AS Logic Data Book (1995)agnamotreg metaya	SDAD001C
BCT BiCMOS Bus-Interface Logic Data Book (1994)	SCBD001B
Boundary-Scan Logic IEEE Std 1149.1 (JTAG) Data Book (1997)	
CBT Bus Switches Crossbar Technology Data Book (1996)	SCDD001A
CDC Clock-Distribution Circuits Data Book (1996)	SCAD004A
F Logic Data Book (1994)	SDFD001B
GTL, BTL, and ETL Logic Data Book (1997)	SCED004
High-Performance FIFO Memories Data Book (1996)	
High-Performance FIFO Memories Designer's Handbook (1996)	SCAA012A
High-Speed Memory Interface Logic Data Book (1997)	SCED001
IEEE Std 1149.1 (JTAG) Testability Primer (1997)	SSYA002C
Low-Voltage Logic Data Book (1996)	SCBD003B
LVC Designer's Guide (1996)	

Example:



Standard Prefix

Example: SNJ - Conforms to MIL-PRF-38535 (QML)

Military (54) or Commercial (74)

3 **Family**

Example: Blank - Transistor-Transistor Logic ABT - Advanced BiCMOS Technology ABTE - Advanced BiCMOS Technology/ Enhanced Transceiver Logic AC/ACT – Advanced CMOS Logic AHC/AHCT - Advanced High-Speed CMOS Logic ALS - Advanced Low-Power Schottky Logic AS - Advanced Schottky Logic ALVC - Advanced Low-Voltage CMOS Technology BCT - BiCMOS Bus-Interface Technology CBT - Crossbar Technology CDC - Clock-Distribution Circuits F-F Logic FB - Backplane Transceiver Logic/Futurebus+ GTL - Gunning-Transceiver Logic HC/HCT – High-Speed CMOS Logic LS - Low-Power Schottky Logic LV - Low-Voltage HCMOS Technology LVC - Low-Voltage CMOS Technology LVT - Low-Voltage BiCMOS Technology S - Schottky Logic SSTL - Series-Stub Terminated Logic

Special Features

Example: Blank = No Special Features D - Level-Shifting Diode (CBTD) H - Bus Hold (ALVCH)

R - Damping Resistor on Inputs/Outputs (LVCR) S - Schottky Clamping Diode (CBTS)

U - Unbuffered Output (AHCU)

5 Bit Width

Example: Blank = Gates, MSI, and Octals 1G - MicroGate (Single Gate) 8 - Octal IEEE 1149.1 (JTAG) 16 - Widebus™ (16, 18, and 20 Bit) 18 - Widebus™ IEEE 1149.1 (JTAG) 32 - Widebus+™ (32 and 36 Bit)

Options ----- MOANT

Example: Blank = No Options 2 - Series-Damping Resistor on Outputs 4 – Level Shifter 25 – 25-Ω Line Driver

Function

Example: 244 - Noninverting Octal Buffer/Driver 374 – Octal D-Type Flip-Flop 573 - D-Type Transparent Latch 5/3 – D-Type Transparent Latch 640 – Inverting Octal Transceiver

Device Revision

Example: Blank = No Revision Letter Designator A–Z

Packages

Example: D, DW - Small-Outline Integrated Circuit (SOIC) DB, DL - Shrink Small-Outline Package (SSOP) DBB, DGV - Thin Very Small-Outline Package (TVSOP) DBV - Small-Outline Transistor Package DGG, PW - Thin Shrink Small-Outline Package (TSSOP) FK - Leadless Ceramic Chip Carrier FN - Plastic Leaded Chip Carrier GB - Ceramic Pin Grid Array HFP, HS, HT, HV - Ceramic Quad Flat Package J, JT - Ceramic Dual-In-Line Package N, NT - Plastic Dual-In-Line Package (DIP) PAG, PAH, PCA, PCB, PM, PN, PZ -Plastic Thin Quad Flat Package PH. PQ. RC - Plastic Quad Flat Package W, WA, WD – Ceramic Flat Package

10 Tape and Reel

Example: LE - Left Embossed (Required for DB and PW Packages) R - Standard (Required for DGG, DBB, DGV, and DBV; Optional for D, DL, and DW Packages)

Device + Package Code (Full Name Symbol)



SSOP Code Abbreviations

or

TSSOP Code Abbreviations

Device Name →	Name Rule or SSOP	Name Rule TSSOP
74AC***	AC***	AC***
74AC11***		
74ACT***		
74ACT1***		
74ACT11***		
CDC***		CK***
SN64BCT***		
SN64BCT2***		
SN64BCT25***	DCT25***	
SN64BCT29***	DCT29***	
SN74ABT***		
SN74ABT***-S	ABT***-S	AB***-S
SN74ABT16***		AH***
SN74ABT18***		
SN74ABT2***	ABT2***	AA***
		AF***
	ABT8***	AG***
SN74ABTH***	ABTH***	AK***
SN74ABTH16***		
SN74ABTH18***	ABTH18***	AL***
SN74AHC***	AHC***	HA***
SN74AHCT***	AHCT***	HB***
SN74AHCU***	AHCU***	HD***
SN74ALS***	ALS***	G***
SN74ALVCH16***	ALVCH16***	VH***
SN74ALVCHG16***	ALVCHG16*** .	VG***
SN74AS***	74AS***	AS***
SN74BCT***		
SN74BCT11***	BCT11***	BB***
SN74BCT2***	BCT2***	BA***
SN74BCT25***	BCT25***	BC***
SN74BCT29***	BCT29***	BD***
SN74BCT8***	BCT8***	BG***
SN74CBT***	CBT***	CT***
SN74CBT16***	CBT16***	CY***

Device Name → N	ame Rule or P	lame Rule TSSOP
SN74CBT3***	. CBT3***	. CU***
SN74CBT6***		
SN74CBTD***	. CBTD***	. CD***
SN74CBTD3***		
SN74CBTS***	. CBTS***	. CS***
SN74CBTS3***	. CBTS3***	. CR***
SN74F***	74F***	. F*** Oximexa
SN74H***	74H***	. H***
SN74HC***	HC***	. HC***
SN74HCT***	HCT***	. HT***
SN74HCU***	HCU***	. (U)***
SN74HCU***	HCU***	. HU***
SN74LS***	74LS***	. LS***
SN74LV***		. LV***
SN74LVC***		
SN74LVC16***	LVC16***	. LD***
SN74LVC2***	LVC2***	. LE***
SN74LVC4***	LVC4***	. LJ***
SN74LVCC3***	LVCC3***	. LH***
SN74LVCC4***	LVCC4***	. LG***
SN74LVCH***	LVCH***	. LCH***
SN74LVCH16***	LVCH16***	. LDH***
SN74LVCR2***	LVCR2***	. LER***
SN74LVCU***	LVCU***	. LCU***
SN74LVT***	LVT***	. LX***
SN74LVT***-S	LVT**-S*	. LX***-S
SN74LVT18***	LVT18***	
SN74LVT2***		. LY***
SN74LVTH***	LVTH***	. LXH***
SN74LVTR***		. LXR***
SN74LVTT***	LVTT***	. LXT***
SN74LVTZ***		. LXZ***
SN74LVU***	LVU***	. LU***
SN74S***	745***	

TABLE OF CONTENTS

SECTION 1 - LOGIC OVERVIEW 1-1
Advanced Bus Interface and Standard Logic
Advanced System Logic (ASL) Advanced Bus Interface (ABI) Contacts/Information
Product Life Cycle
CMOS Is Growing, Bipolar Is Shrinking
Worldwide CMOS Logic Market
Packaging Options
Bus-Switch Package Options
Family Positioning
Advanced High-Speed CMOS – AHC/AHCT
Key Comparisons AHC/HC/VHC
AHC/AHCT Product Offerings
AHC/AHCT MicroGates
AHC/AHCT MicroGate Product Offerings
Advanced BiCMOS Technology – ABT
Advanced Biolivios Technology – ABT ABT is Fast!
ABT Has Lower Ground Bounce!
ABT Has Lower Ground Bouncei 1–20 ABT Has Power-Up 3-State! 1–21
Why ABT Rather Than FCT?
TI Provides a Faster, More Complete Roadmap to Lower Voltages!
Crossbar Technology – CBT
CBT Bus-Exchange Switches
IC Basics – Comparison of Switching Standards
Low-Voltage Logic 3.3-V Competitive Analysis
Complete Low-Voltage Market Coverage and Standardization
Low-Voltage Technology – LVT
Low-voitage Civios – Lvo
Low voitage - Lv
Advanced Low-Voltage CMOS – ALVC
Old Solution for Defining CMOS Inputs
Bus-Hold Input Characteristics
Logic With Bus Hold1–35
Damping Resistors
TI Damping Resistors vs. IDT Balanced Drive
IC Basics Comparison of Backplane Switching Standards
What is GTL?
Advantages of GTL
Design Considerations
What Does TI Offer in IEEE 1149.1 (JTAG) Silicon Solutions?
The Boundary-Scan Idea1–43
End-Equipment Designing With JTAG Boundary Scan
FIFO Product Portfolio1–45

STRETHON TO BURNE

SECTI	ON 2 - FUNCTIONAL INDEX	2-1
	Buffers/Drivers and Bus Transceivers	2-5
	Buffers/Drivers	2-5
	Bus Transceivers	2-7
	Bus Transceivers With Registers	2-8
	Bus Transceivers With Latches	
	Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)	
	Parity Transceivers	
	Non-TTL Transceivers	
	Flip-Flops and Latches	
	Flip-Flops	
	Latches	
	Bus-Termination Arrays	
	Bus-Termination Arrays	
	Bus Switches	
	Bus Switches	
	Counters	
	Synchronous Counters – Positive Edge Triggered	
	Asynchronous Counters (Ripple Clock) – Negative Edge Triggered	
	Other Counters	
	Shift Registers	
	Shift Registers	
	Encoders, Data Selectors/Multiplexers, and Bus Exchangers	
	Encoders, Data Selectors/Multiplexers, and Bus Exchangers	
	Decoders/Demultiplexers and Oscillators	
	Decoders/Demultiplexers	
	Oscillators	
	Comparators and Parity Generators/Checkers	
	Comparators	
	Parity Generators/Checkers	
	Arithmetic Circuits eotranomenud tugni sloF-aut	2-22
	Adders	
	Arithmetic Logic Units	
	Dividers/Multipliers	
	Monostable Multivibrators	
	Gates S.JTE) el iarrivi	
	Positive-AND Gates	7-20
	Positive-NAND Gates	
	Positive-OR Gates	
	Positive-NOR Gates sehi mod-gab mod en	
	XOR Gates	2-24
	XNOR Gates	2-25
	AND/NOR Gates	2-25
	Hex Inverters/Noninverters and Delay Elements	2-26
	Hex Inverters/Noninverters	
	Delay Elements	2-26

TABLE OF CONTENTS (continued)

SECTION 2 (co	ontinued)	
II S	49.1 (JTAG) Boundary-Scan Logic Devices EEEE 1149.1 Boundary-Scan Logic Scan-Support Devices emories	2-28
	First-In, First-Out (FIFO) Memories	
SECTION 3 - F	FUNCTIONAL CROSS-REFERENCE	3-1
SECTION 4 - D	DEVICE SELECTION QUIDE	4-1
ABT – Ad	Advanced BiCMOS Technology	4-{
	TL - Advanced BiCMOS Technology/Enhanced Transceiver Logic	
	- Advanced CMOS Logic	
	ICT – Advanced High-Speed CMOS Logic	
	dvanced Low-Voltage BiCMOS	
	dvanced Low-Power Schottky Logic	
	Advanced Low-Voltage CMOS Technology	
	Ivanced Schottky Logic	
	BICMOS Bus-Interface Technology	
	- 64-Series BiCMOS Technology	
	us-Termination Arrays	
	+ – Backplane Transceiver Logic	
	ast Logic	
	First-In, First-Out Memories	
	Gunning-Transceiver-Logic Technology	
	- High-Speed CMOS Logic	
	49.1 (JTAG) Boundary-Scan Logic Devices	
	w-Power Schottky Logic	
	w-Voltage CMOS Technology	
	ow-Voltage CMOS Technology	
	ow-Voltage BiCMOS Technology	
S - Scho	ottky Logic	4–87
	Series-Stub Terminated Logic	
TTL - Tra	ransistor-Transistor Logic	4–91

TABLE OF CONTENTS (continued)

	IEEE 1149.1 (o p.ko.) Entraciny-Sean Logio Sean-Support Devices
	SCTON 3 - FUNCTIONAL CROSS-PETERBUCK
V-3	
58P	

LOGIC OVERVIEW	1
FUNCTIONAL INDEX	2
	\$
FUNCTIONAL CROSS-REFERENCE	3
DEVICE SELECTION GUIDE	4

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SECTION 1 LOGIC OVERVIEW

CONTENTS

Advanced Bus Interface and Standard Logic	1–5
Advanced System Logic (ASL) Advanced Bus Interface (ABI) Contacts/Information	
Product Life Cycle	1–7
CMOS Is Growing, Bipolar Is Shrinking	1–8
Worldwide CMOS Logic Market	
Packaging Options	
Bus-Switch Package Options	
Family Positioning	1–12
Advanced High-Speed CMOS – AHC/AHCT	1–13
Key Comparisons AHC/HC/VHC	
AHC/AHCT Product Offerings	1–15
AHC/AHCT MicroGates	
AHC/AHCT MicroGate Product Offerings	1–17
Advanced BiCMOS Technology - ABT	
ABT is Fasti	
ABT Has Lower Ground Bouncel	1–20
ABT Has Power-Up 3-Statel	1–21
Why ABT Rather Than FCT?	
TI Provides a Faster, More Complete Roadmap to Lower Voltages!	
Crossbar Technology - CBT	
CBT Bus-Exchange Switches	1–25
IC Basics - Comparison of Switching Standards	
Low-Voltage Logic 3.3-V Competitive Analysis	
Complete Low-Voltage Market Coverage and Standardization	1–28
Low-Voltage Technology – LVT	
Low-Voltage CMOS – LVC	
Low Voltage – LV	
Advanced Low-Voltage CMOS – ALVC	
Old Solution for Defining CMOS Inputs	
Bus-Hold Input Characteristics	
Logic With Bus Hold	
Damping Resistors	
TI Damping Resistors vs. IDT Balanced Drive	
IC Basics Comparison of Backplane Switching Standards	
What is GTL?	
Advantages of GTL	
Design Considerations	1-41
What Does TI Offer in IEEE 1149.1 (JTAG) Silicon Solutions?	
The Boundary-Scan Idea	
End-Equipment Designing With JTAG Boundary Scan	1–44
FIFO Product Portfolio	1_15

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STMITHOU

Popular Microsoft Productions
Basics - Comparison of Switching Standards
VJ - angloV vu l

Advanced Bus Interface & Standard Logic

INSTRUMENTS FEXAS

One Stop Logic Shop!

Advanced System Logic Products



Advanced System Logic (ASL) Advanced Bus Interface (ABI) Contacts/Information

Product Information Center: 972/644-5580

ASL Fax: 903/868-5980

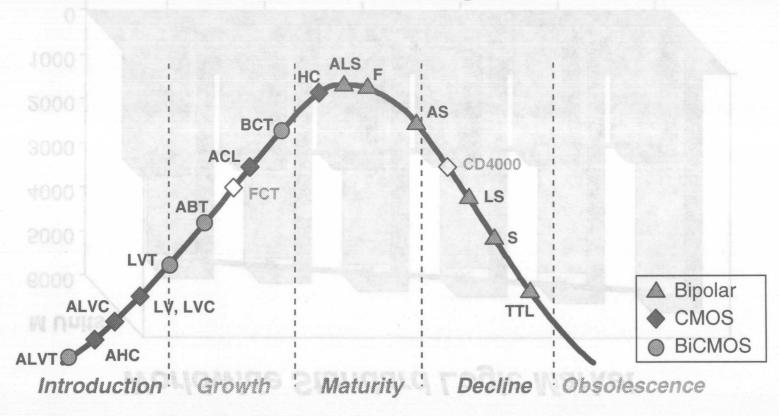
TI Home Page: http://www.ti.com

ASL Home Page: http://www.ti.com/sc/docs/asl/home.htm

Datasheets: http://www.ti.com/sc/docs/psheets/pids.htm

Texas Instruments
P.O. Box 84, M/S 835
Sherman, TX 75091

Product Life Cycle

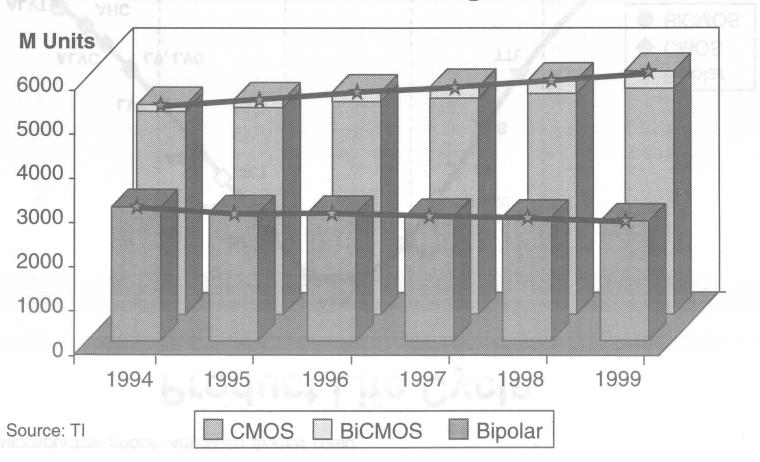


- TI remains committed to be the last supplier in the older families.
- Investment levels for new products are at an all-time high, while end-equipment requirements are accelerating new product introduction.



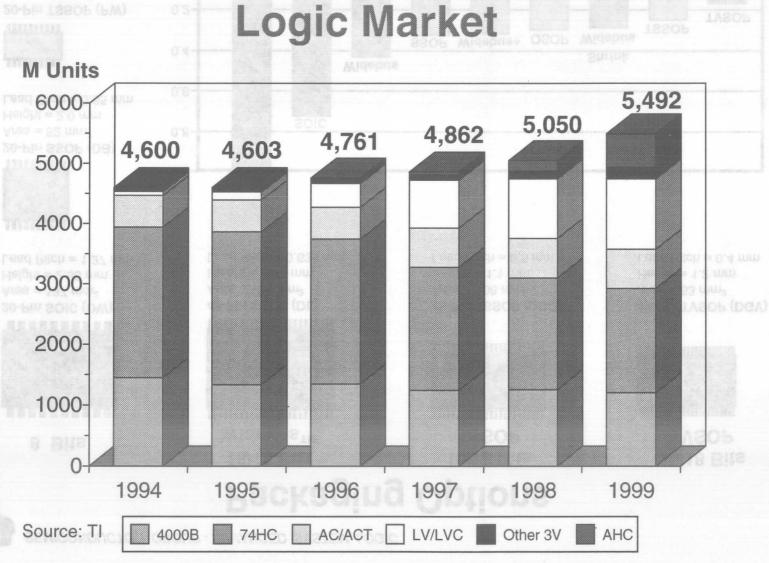
• Investment levels CMOS Is Growing, Investment levels CMOS Is Growing,

Worldwide Standard Logic Market





Worldwide CMOS Logic Market

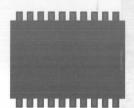




SEMICONDUCTOR GROUP - ADVANCED SYSTEM LOGIC

Packaging Options

8 Bits



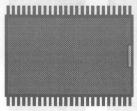
20-Pin SOIC (DW) Area = 137 mm² Height = 2.65 mm Lead Pitch = 1.27 mm



20-Pin SSOP (DB) Area = 62 mm² Height = 2.0 mm Lead Pitch = 0.65 mm



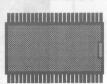
20-Pin TSSOP (PW) Area = 46 mm² Height = 1.1 mm Lead Pitch = 0.65 mm 16/18 Bits Widebus™



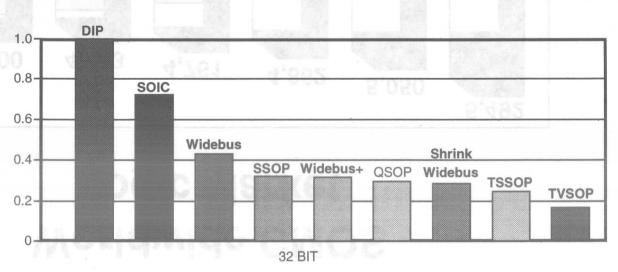
48-Pin SSOP (DL) Area = 171 mm² Height = 2.74 mm Lead Pitch = 0.635 mm 16/18 Bits TSSOP



48-Pin TSSOP (DGG) Area = 108 mm² Height = 1.1 mm Lead Pitch = 0.5 mm 16/18 Bits TVSOP



48-Pin TVSOP (DGV) Area = 63 mm² Height = 1.2 mm Lead Pitch = 0.4 mm

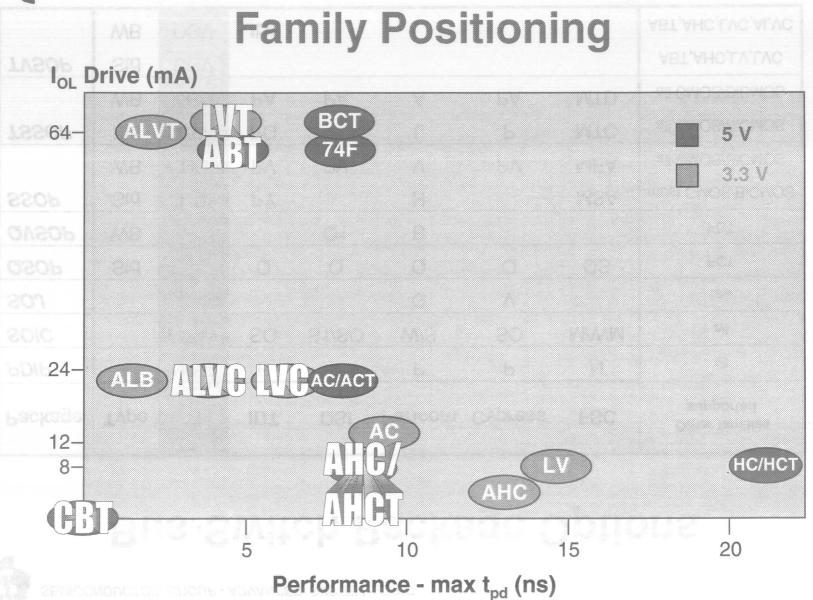


Bold indicates TI TTL/CMOS logic packages.

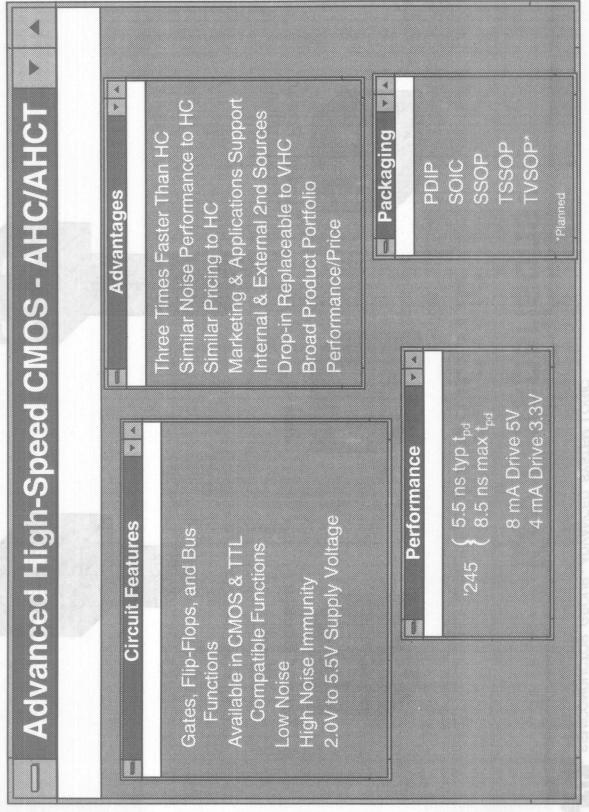
(TI package designators)

Bus-Switch Package Options

Package	Туре	TI	IDT	QSI	Pericom	Cypress	FSC	Other families supported
PDIP		N/NT	Р	Р	Р	Р	N	all
SOIC		D/DW	SO	S1/S0	W/S	SO	M/WM	all
SOJ	***************************************				G	V		few
QSOP	Std		Q	Q	Q	Q	QS	FCT
QVSOP	WB		***************************************	Q1	В			FCT
SSOP	Std	DB	PY		Н		MSA	most CMOS/BiCMOS
	WB	DL	PV	PV	V	PV	MEA	all CMOS/BiCMOS
TSSOP	Std	PW	PG		L	P	MTC	all CMOS/BiCMOS
or	WB	DGG	PA	PA	Α	PA	MTD	all CMOS/BiCMOS
TVSOP	Std	DGV			***************************************			ABT,AHC,LV,LVC
	WB	DGV	tbd					ABT,AHC,LVC,ALVC

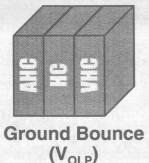


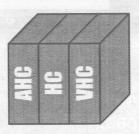




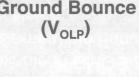


Key Comparisons AHC/HC/VHC

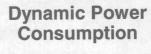


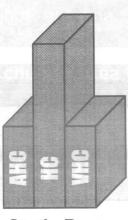




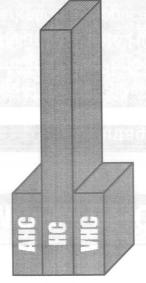








Static Power Consumption



Propagation Delay



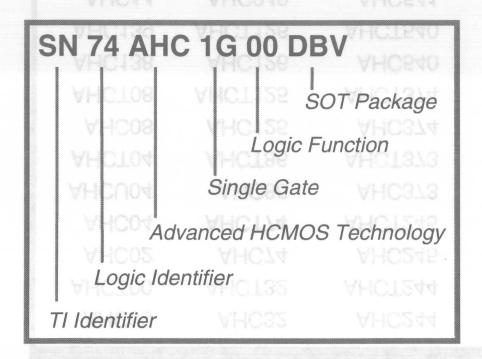
AHC/AHCT Product Offerings

	Rele	ased		Planned
AHC00	AHC32	AHC244	AHC573	AHCT138
AHCT00	AHCT32	AHCT244	AHCT573	AHCT139
AHC02	AHC74	AHC245	AHC574	AHC157
AHC04	AHCT74	AHCT245	AHCT574	AHCT157
AHCU04	AHC86	AHC373	♦ 20uA s	AHC158
AHCT04	AHCT86	AHCT373	4 00	AHCT158
AHC08	AHC125	AHC374	* +/-8INA	AHC257
AHCT08	AHCT125	AHCT374	+ 3.5 ns i	AHCT257
AHC138	AHC126	AHC540	◆ ASIC #	AHC258
AHC139	AHCT126	AHCT540	1 0000	AHCT258
AHC14	AHC240	AHC541	+ Simplifi	AHCT02
AHCT14	AHCT240	AHCT541		

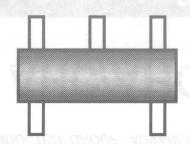
1813 y



AHC/AHCT MicroGates



- ♦ Simplifies circuit routing
- ♦ ASIC modification
- ♦ 3.5 ns typ propagation delay
- ♦ +/-8mA output drive
- ♦ 20uA static current
- ◆ CMOS (AHC) and TTL (AHCT) versions
- Compatible with Toshiba's TC7SH/SHTxx series
- ♦ Volume production: now



Cross-Reference (examples)

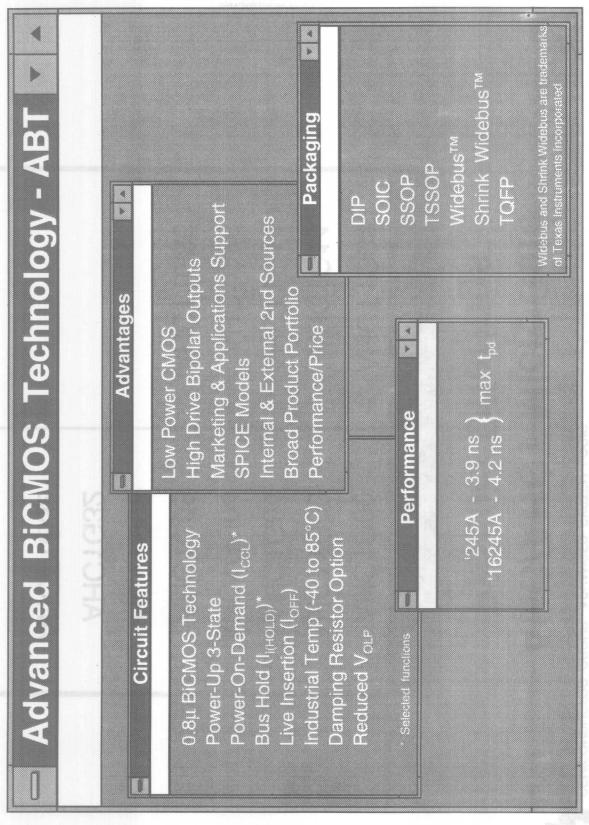
Texas Instruments	Toshiba
SN74AHC1G00DBV	TC7SH00F
SN74AHCT1G00DBV	TC7SHT00F
SN74AHC1GU04DBV	TC7SHU04F



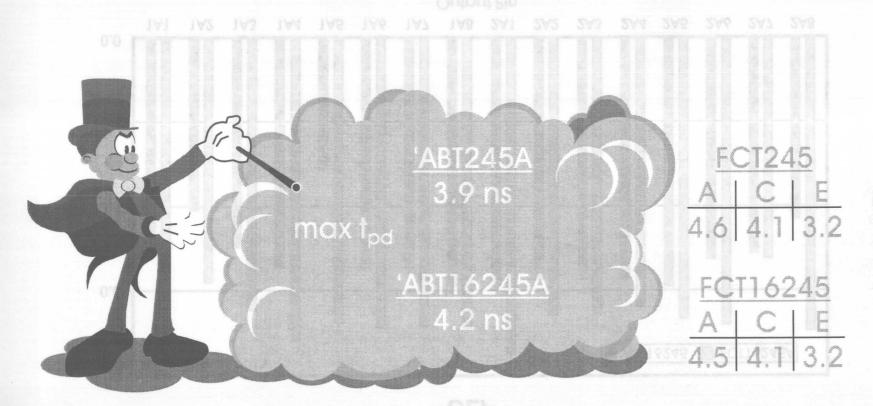
AHC/AHCT MicroGate Product Offerings

Released	Planned
AHC1G00	AHCT1G04
AHCT1G00	AHC1G14
AHC1G04	AHCT1G14
AHC1GU04	AHC1G86
AHC1G08	AHCT1G86
AHCT1G08	Advantages
AHC1G32	
AHCT1G32	al elemnonogy





ABT Is Fast!



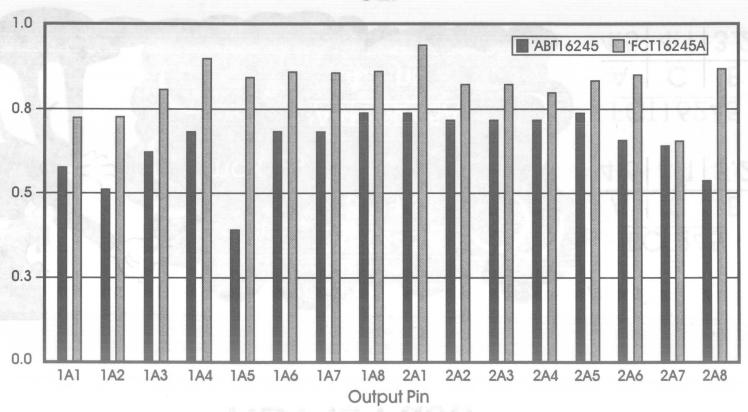
ABT is price competitive with FCT!



SEMICONDUCTOR GROUP - ADVANCED SYSTEM LOGIC

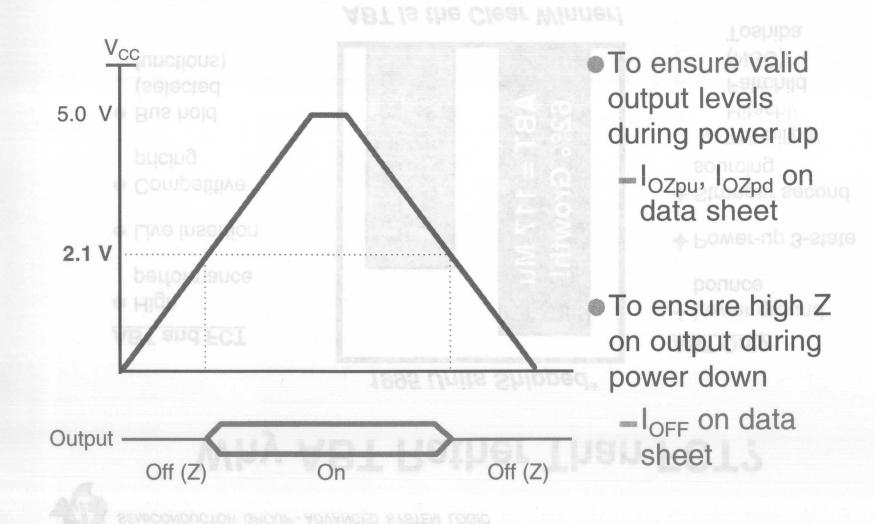
ABT Has Lower Ground Bounce!

VOLP



 V_{CC} = 5.5V V, C_L = 50 pF, R_L = 500 Ω , 15 Outputs Switching, Freq = 1 MHz, T_A = 25°C, V_{INL} = 0.5V, V_{INH} = 2.5V

ABT Has Power-Up 3-State!



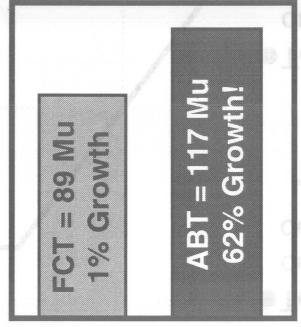


Why ABT Rather Than FCT?

ABT and FCT

- High performance
- Live insertion
- Competitive pricing
- Bus hold (selected functions)

1995 Units Shipped* DOMEL GOMU



ABT Is the Clear Winner!

ABT Only

- Lower ground bounce
- ♦ Power-up 3-state
- Stronger second sourcing
 - TI/Philips/ Hitachi/ Fairchild (NSC)/ Toshiba

TI provides a complete roadmap to lower voltages!

*Source: Insight Onsite



TI Provides a Faster, More Complete Roadmap to Lower Voltages!

Speed

```
ALB16
                2.0 ns
                  2.4 ns
ALVT16
                           3.6 ns
ALVC16
LVT
                              4.0 ns
LVC16
                                       5.2 ns
FCT163-C
                               4.1 ns
FCT163-A
                                    4.8 ns
                                                 6.5 ns
FCT163
```

Drive

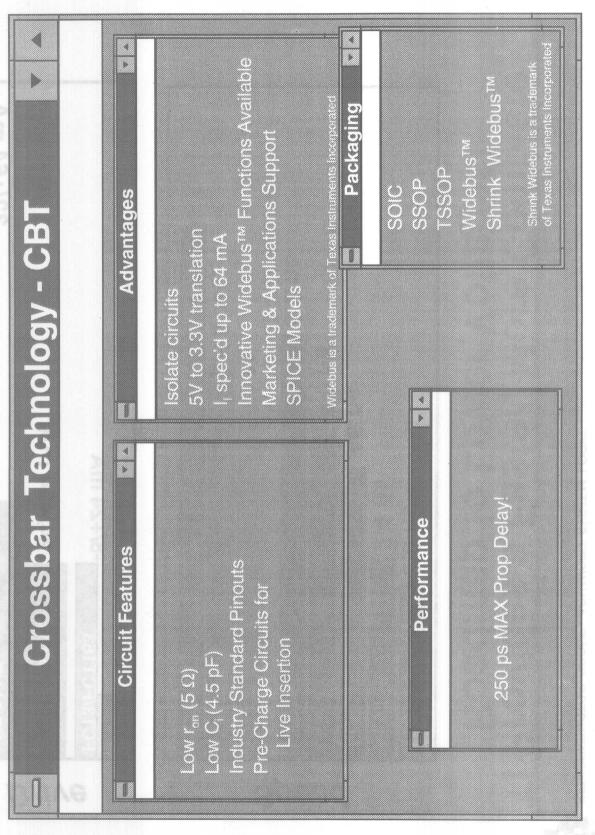
```
FCT3/FCT168 -8/+24 mA*

ALVC/ALB/LVC -24/+24 mA*

LVT/ALVT -32/+64 mA

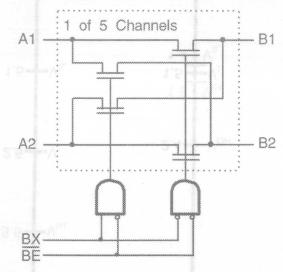
* ALB: -25/+25 mA
```





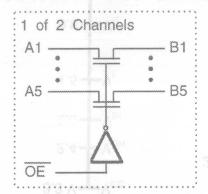
CBT Bus-Exchange Switches

CBT3383 BUS EXCHANGER



- Simple FET Switches
- Functionally Equivalent To: QS3383 and QS3384
- Industry Standard Pinouts ('244, '245)
- Widebus[™] Functions Available
- Fine-Pitch Packaging Options (SOIC, SSOP, TSSOP, Widebus, Shrink Widebus™)
- Octals and Widebus available NOW!

CBT3384A BUS SWITCH



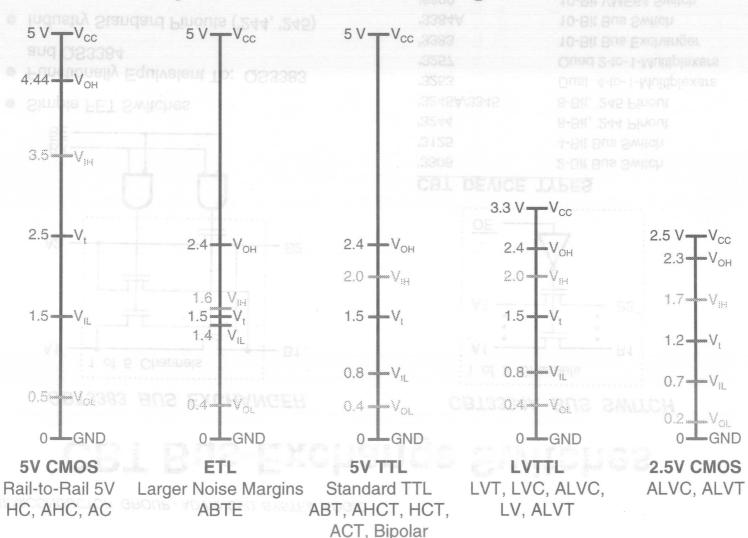
CBT DEVICE TYPES

CDI DEVICE	- III LO
'3306	2-Bit Bus Switch
'3125	4-Bit Bus Switch
'3244	8-Bit, '244 Pinout
'3245A/3345	8-Bit, '245 Pinout
'3253	Dual 4-to-1-Multiplexers
'3257	Quad 2-to-1-Multiplexers
'3383	10-Bit Bus Exchanger
'3384A	10-Bit Bus Switch
'6800	10-Bit VME64 Switch
'16209	18-Bit Bus Exchanger
16211	24-Bit Bus Switch
'16212/16213	24-Bit Bus Exchanger
'16214	12-Bit 3-to-1 Bus Select
¹ 16244	16-Bit Bus Switch

Widebus and Shrink Widebus are trademarks of Texas Instruments Incorporated

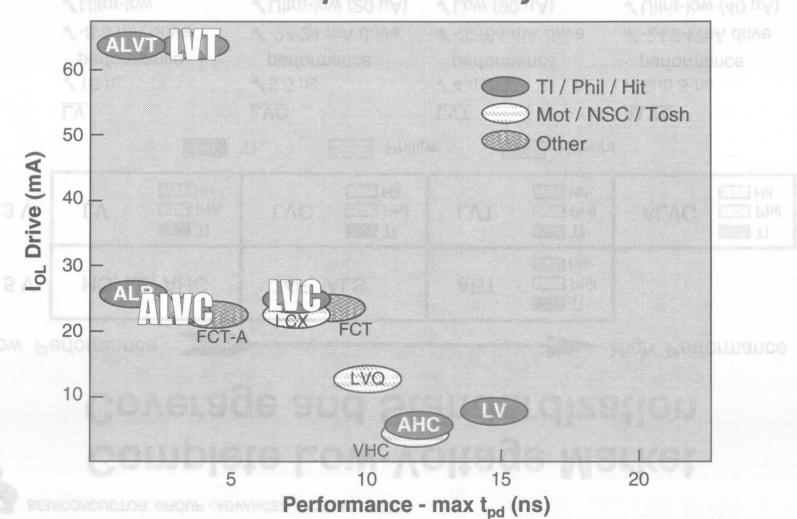
SSOP, TSSOP, Widebus, Shrink IC Basics

Comparison of Switching Standards





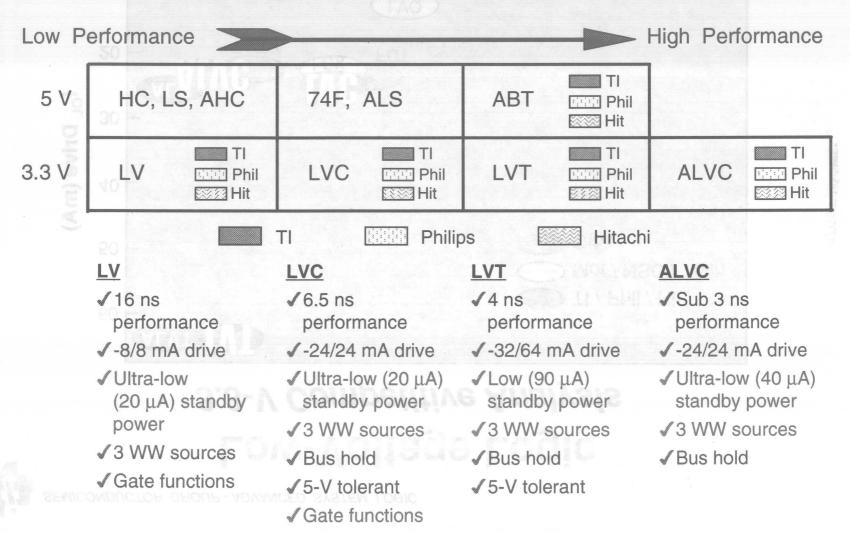
Low-Voltage Logic 3.3-V Competitive Analysis



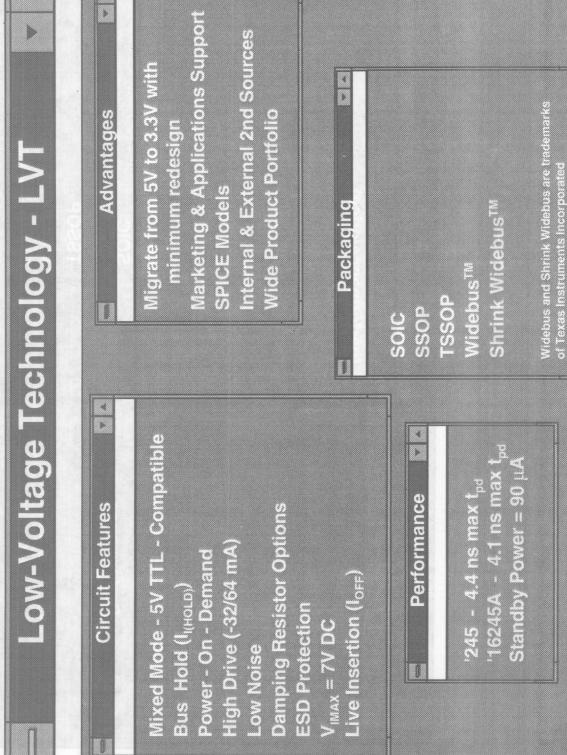


SEMICONDUCTOR GROUP - ADVANCED SYSTEM LOGIC - 11193 (1991)

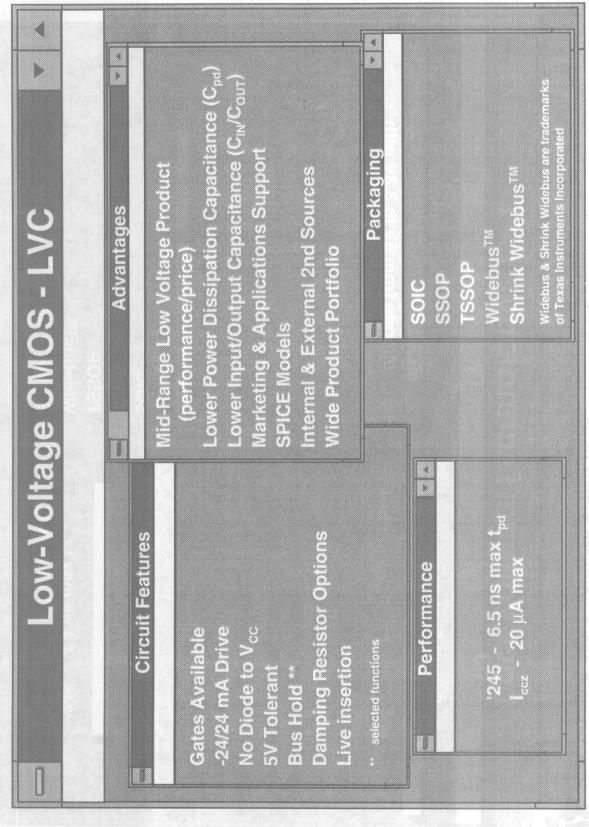
Complete Low-Voltage Market Coverage and Standardization



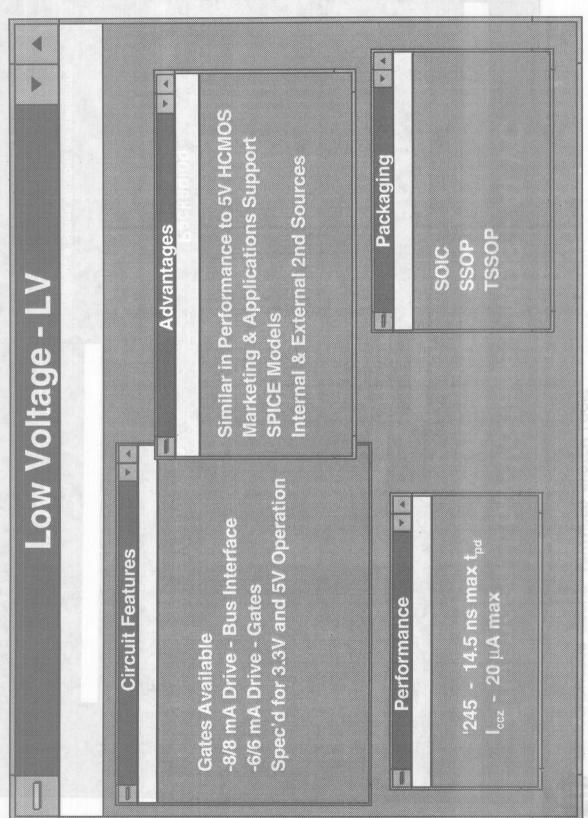




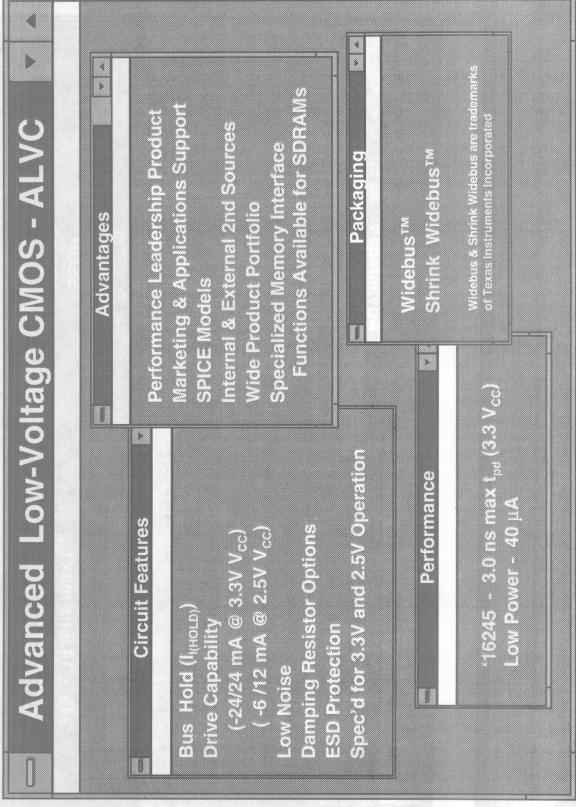






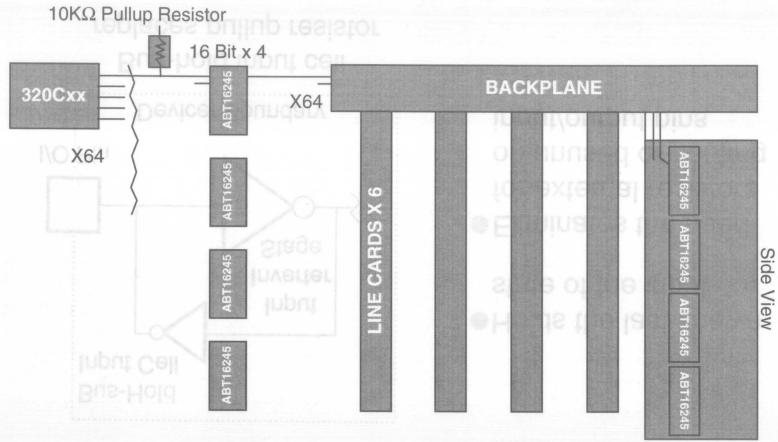






Jis

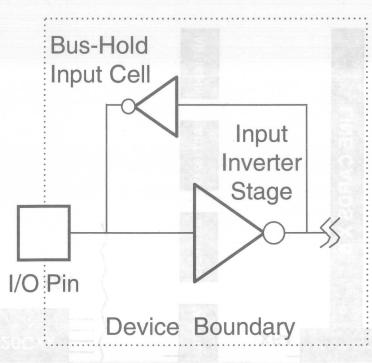
Old Solution for Defining CMOS Inputs



- 448 pullup resistors needed to protect against floating inputs
- Additional cost = \$\$
- Additional board space
- Additional power consumption (In this case, 1.08W)



Bus-Hold Input Characteristics



Bus-hold input cell replaces pullup resistor

- Holds the last known state of the input
- Eliminates the need for external resistors on unused or floating input/output pins

Logic With Bus Hold

ABTH

- 12 devices with bus hold

LVT

- All LVT devices have bus hold

Name change to LVTH in progress

LVCH

- 14 devices with bus hold

ALVCH - All devices have bus hold

(>40 devices)

AHCH/AHCTH - Bus hold planned on Widebus™ devices

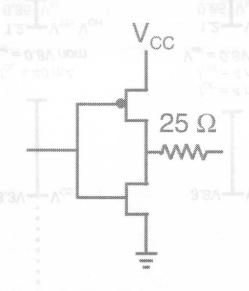
Damping Resistors

- WHY: 1. Damping resistors limit current, thereby reducing noise from undershoot / overshoot
 - 2. Help in line termination (reduce ringing / line reflection to improve signal quality)

eg: ABT<u>2</u>245 ABT16<u>2</u>245 Extra "2" in device name indicates damping resistor

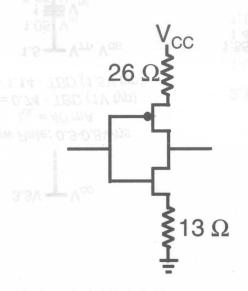


TI Damping Resistor vs. IDT Balanced Drive



TI's placement of the series-damping resistor meets both goals:

- **♦** Limit current
- → Help in line termination



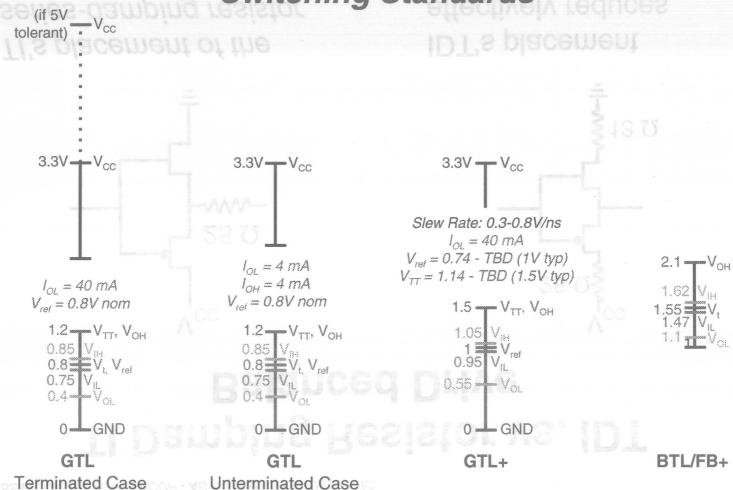
IDT's placement effectively reduces current only. This is not the method preferred for line termination.



SEMICONDUCTOR GROUP - ADVANCED SYSTEM LOGIC

terminal Cn Basics ine termin

Comparison of Backplane Switching Standards



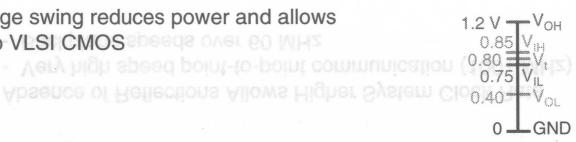


GTL transceMhatsis GTL 5 st per bit as BTL drivers

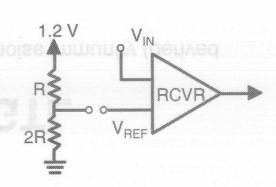
Driver is an open-drain n-channel CMOS transistor



Reduced voltage swing reduces power and allows integration into VLSI CMOS



Receiver stage is a differential input with external V_{REF} set at 0.8V. V_{REF} is derived from simple R/2R voltage divider of 1.2V pull-up.



Advantages of GTL

Noise:

External V_{REF} provides common-mode noise immunity (derived

from 1.2V pullup).

Low signal amplitude reduces EMI

Speed:

Absence of Reflections Allows Higher System Clock Rate

- Very high speed point-to-point communication (100+ MHz)

Diedusion into-Backplane speeds over 60 MHz

Power:

High-speed, low-power backplane alternative to BTL or ECL

Power Comparison (160 active I/Os)

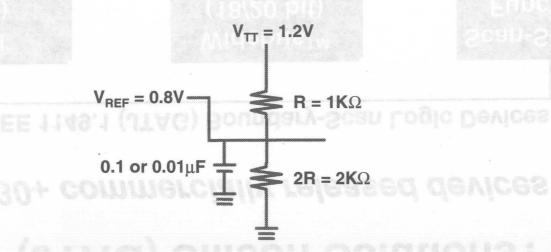
Technology	Power (watts)	Termination
ECL 10K	20	25 Ω to 3.0V
-dBLFn-chann	el CMQ15 transi	16.5 Ω to 2.0V
GTL	1.5	50 Ω to 1.2V

Cost:

GTL transceivers are less than half the cost per bit as BTL drivers of comparable speeds.

Design Considerations

- \bullet V_{TT} (1.2/1.5V) must be regulated from V_{CC}
- V_{REF} must be generated from (1.2/1.5V) V_{TT}
- Add bypass capacitors to regulate the 0.8V V_{REF}



Need both 3.3V_{CC} and 5V_{CC} power supply on the 'GTL16612

Linear Technology makes some regulators
- 1.2V LT1086 2 amps, GTL+ (1.5V) LT1587-1.5

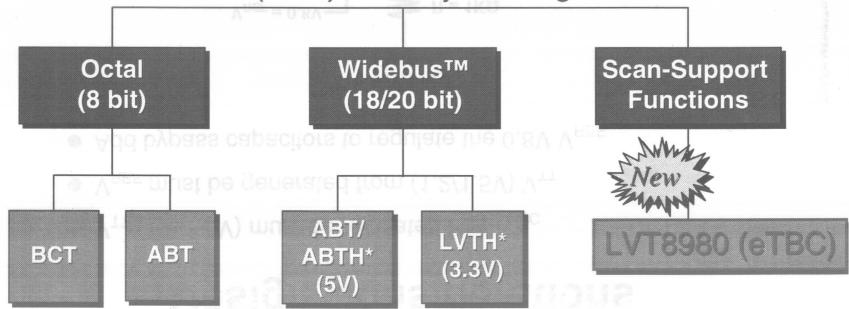


SEMICONDUCTOR GROUP - ADVANCED SYSTEM LOGIC

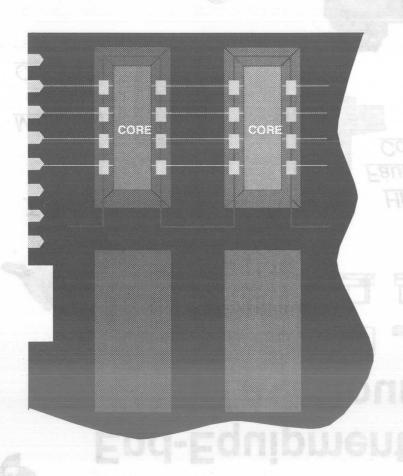
What Does TI Offer in IEEE 1149.1 (JTAG) Silicon Solutions?

30+ commercially released devices

IEEE 1149.1 (JTAG) Boundary-Scan Logic Devices



The Boundary-Scan Idea



- Scan provides a means to arbitrarily observe test results and source test stimulus
 - Scan method requires minimal on-chip/board resources (pins/nets)

SEMICONDUCTOR GROUP - ADVANCED SYSTEM LOGIC

End-Equipment Designing with JTAG Boundary Scan



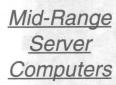
Networking







Telecom

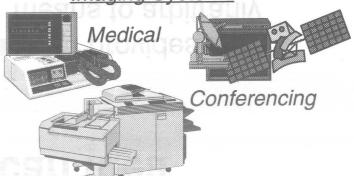




High-End Fault-Tolerant **Computers**



Imaging Systems

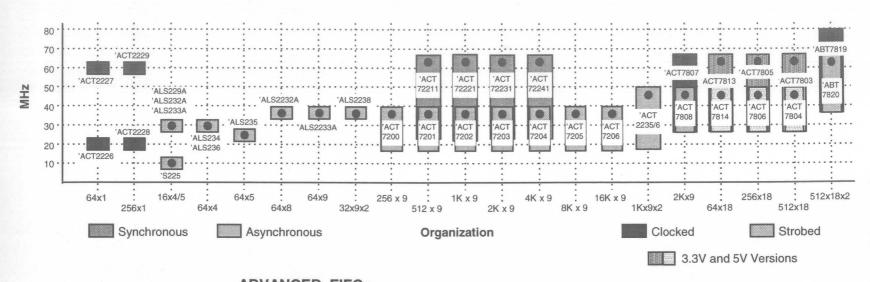


Copiers

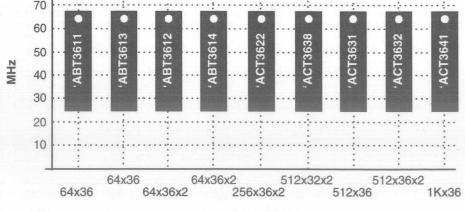




FIFO Product Portfolio







Organization

- Multiple Speed Sorts
- Unidirectional and Bidirectional
- Advanced Fine-Pitch Packaging





LOGIC OVERVIEW	1
FUNCTIONAL INDEX	2
	<u> </u>
FUNCTIONAL CROSS-REFERENCE	3
DEVICE SELECTION GUIDE	4

XEGHT JAMOSTONUT

SECTION 2 FUNCTIONAL INDEX

CONTENTS

Buffers/Drivers and Bus Transceivers
Buffers/Drivers
Bus Transceivers
Bus Transceivers With Registers
Bus Transceivers With Latches
Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)
Parity Transceivers
Non-TTL Transceivers
Flip-Flops and Latches
Flip-Flops
Latches
Bus-Termination Arrays2–15
Bus-Termination Arrays
Bus Switches
Bus Switches
Counters
Synchronous Counters – Positive Edge Triggered
Asynchronous Counters (Ripple Clock) - Negative Edge Triggered2-17
Other Counters
Shift Registers
Shift Registers
Encoders, Data Selectors/Multiplexers, and Bus Exchangers
Encoders, Data Selectors/Multiplexers, and Bus Exchangers2-19
Decoders/Demultiplexers and Oscillators
Decoders/Demultiplexers
Oscillators
Comparators and Parity Generators/Checkers
Comparators
Parity Generators/Checkers
Arithmetic Circuits
Adders 2–22
Arithmetic Logic Units
Dividers/Multipliers
Monostable Multivibrators
Gates
Positive-AND Gates
Positive-NAND Gates 2–23
Positive-OR Gates 2–24
Positive-NOR Gates 2–24
XOR Gates 2–25
XNOR Gates 2–25 XNOR Gates 2–25
AND/NOR Gates 2–25 AND/NOR Gates 2–25
AND/NOR Gales2-25

CONTENTS (continued) Hex Inverters/Noninverters 2–26

FUNCTIONAL INDEX

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers

DESCRIPTION	OUTPUT	TYPE										TEC	HNOLO	GY								
DESCRIPTION	COTPOT	ITTE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
Quad	3S	'125	~		V	V			V	V					V	V		V	~	V	V	- u- i
Quad of suspension in the	33	'126	4	CE SASSES	V	MOSO-L	DIDS SCA	STEERED (4	V	(160)	*	n buoon	er bjevus	1	- VA	gespag	~			~	
Noninverting Hex	3S	'365	9-8190							~		*						V				
Miss 20060 Life Mark	3S	'367								V		V					4.	~				
Inverting Hex	3S	'368								V		V						V				
1-to-4 Address Orlvers	3.5	241	V		V	4	V	V	~	~	V		~	V			4-	V			+	
	3S	244	~		V	~	~	V	~	V	~		V.	V.	V	V	+	V	~	~	V	+LVCH
Noninverting Octal		'1244					V					-									-	
Noninverting Octal	33	'541	V		V		V		V	V					V	~	-	~	~		+	
	OC	757	-0,-					V									Dig					
	00	760	-		V		V	~	-					-								
Marie Alexander Dis	00	'240	1		V	V	~	V	~	V	V		V.	V.	~	~		V	V	V	+	
Inverting Octal	3S	'540	V	-	V		V			~					V	~		~	~		+	
	OC	756			V	5.		V									F Fa					
Inverting and Noninverting Octal	38	'230	- 04					V						0,			Ø4,					
43 BH REEK BISH	10	'2240	V		V		V															
Octal	3S	'2241	V			0.											0.,				÷	
With Series Resistors on Output	35	'2244	V		V				V									-3-			+	
mental to ox	22	2541					V							6.			de		-		0	
		'827	V										6	Α,			6,				+	
Noninverting 10 Bit	3S	29827	-		V		V							TA.			-4				0	
annum al annum		'828		6		1			-					A			0.	7			+	
Inverting 10 Bit	3S	'29828					V				-						4				4	-
10 Bit		'2827	V		V																	
With Series Resistors	3S	'2828			V												-					
11 Bit		'5400	V	NOTE:	DIA I	261	5/1965	WO.		F0	- 0	110	5/5/5	1620.1	YOUA	ANCI	WOLG.	180	ROL	FA	rac	OTHE
With Series Resistors	3S	'5401	V		8521	183						100	140000	-	1000	11000					1	

+ New product planned in technology indicated



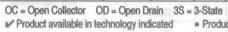
TEXAS INSTRUMENTS

TEXAS INSTRUMENTS

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Buffers/Drivers (continued)

DESCRIPTION	OUTPUT	TYPE										TECI	HNOLO	GY				,				
DESCRIPTION	OUIPUI	TIPE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
12 Bit	38	'5402	V		1																	
With Series Resistors	33	'5403	~																			
		'16241	V				6.							V			+				+	
Noninverting 16 Bit	3S	'16244	V	V		V							V	V			~				V	
		'16541	V		The Control		-6							V			+				V	
Horimoding 10 (9)	- 88 -	'16240	V										V	V			~				V	
Inverting 16 Bit	38	'16540	V	10			0							V		,	+				V	
		'16828	15,		0,				0.					-				+			+	
16 Bit With Series Resistors	38	'162244	V			V											~				+	
17 Bit IEEE P1284	3S	'161284												-	-						+	
N 40 P2	20	'16825	V					6,						1			V					
Noninverting 18 Bit	3S	'16835		-	6.	V		D.									V					
18 Bit With Series Resistors	38	'162825	V		D _i		Ph			4					6.	94,			14		4	
Noninverting 20 Bit	3S	'16827	V					-				-	-	1			V	-	-		-	
20 Bit With Series Resistors	38	'162827	V					O.									~					
1-to-2 Address Drivers	3S	'16830	17		10/		100		PA							-	+					
1-to-2 Address Drivers With Series Resistors	38	'162830	6		1	Ps.	PA .	P _k	Ph	19%			Pari	2/4	17	+,	+	6,	6,	84		+ract
1-to-4 Address Drivers	3S	'16831	D ₀		Ps,	- 14	14	- 0-1	- 14	Ps	25		1	10/2			+	-			+	
1-to-4 Address Drivers With Series Resistors	38	'162831								P ₄		A.					+	A A				



[•] Product available in reduced-noise advanced CMOS (11000 series)

^{*} Product available as a military device only

^{*} Product planned as a military device

⁺ New product planned in technology indicated

TEXAS

DECODIDATION	OUTDIT	TVDE										TEC	HNOLO	GY								
DESCRIPTION	OUTPUT	TYPE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
Noninverting Quad	3S	'243	1 ² 10010	i aveljej	to in ro	nosq-u	~	anced (V	V	(H812)	中超	es buogn	et plane	ad in tex	implogy b	desind					
OC - Open Collector - F	Chan Dr	'245	V		V	V	~	~	V	~			Vo*	V.	V	V		V	V	V	~	+LVCH
		'1245					~							9								
	38	25245	V		V				L					10								2.73 121
	3S	'442								V	1			10								
Nania adia a Ostal		'466	15			-				~			1.5							ļ		
Noninverting Octal	78	'645	1			24	V	V		V			1	- 1				V	V		- Abr	
		'1645	15			1	V						- 6	1			- 5				7	
	00	'621	0				V		*					15								
	oc	'641	100				V	V		V												1
	OC/3S	'639					V	V		10												
	0088	'620	V				V															
		'623	V		V		V		V	V								V	V			
	38	'640	V		V	100	V	V		V			-					V			1	
Inverting Octal		'1640					V			04												
	OC	'642	1		Pa	1	V	1. 1%		V	1							1	10		13	
	OC/3S	'638					V														1	
Octal With Series Resistors on B Port	38	'2245	-	VIB	V	PAL	ALS	48	V	LE	8	LAST	YC	YCA	VHC	AHCT	VEAC	140	HOT	DA	#0	✓LVCF +LVTR
Octal 3.3-V-to-5-V Level Shifter	3S	'4245																			+	
		'863	V																		+	
Noninverting 9 Bit	3S	'29863	100		V		V													1		
Noninverting 10 Bit	3S	'861	V											10.					1		+	
Allega de la companya	-	'16245	V	V		V							V	V			V				V	✓ ABTE
Noninverting 16 Bit	38	'16623	V				-				-			V			200				1	
16 Bit With Series Resistors	38	'162245	V			V							`\				~					∠ LVCF
Noninverting 16-Bit 3.3-V-to-5-V Level Shifter	3S	'164245	VBL	ALB	BOJ.	TAL	ALS	AS		1.8	8	1.18	AC.	ACT	ANG	YHOL	V	же	HOT	ΓA	rac	oun

OC = Open Collector OD = Open Drain 3S = 3-State

Product available in technology indicated

Product available as a military device only

Product

Product available in reduced-noise advanced CMOS (11000 series)
 * Product planned as a military device

⁺ New product planned in technology indicated

TEXAS INSTRUMENTS

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Bus Transceivers (continued)

DESCRIPTION	ОИТРИТ	TYPE										TEC	HNOLO	GY								
DESCRIPTION	OUIPUI	TIPE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
Investing 16 Dit	20	'16640	~										4	~								
Inverting 16 Bit	3S	'16620	14			24							V	V			1					MIACE
Noninverting 18 Bit	3S	'16863	V											V			V					
Inverting 18 Bit	3S	'16864	1	-	-	Fig. 1							6	V			0				a.	NUBBE
Noninverting 20 Bit	38	'16861	h.							-				V					7 11		4	
Noninverting 36 Bit	3S	'32245	V																			

Bus Transceivers With Registers

DESCRIPTION	OUTDUT	TVDE										TEC	HNOLO	GY								
MEDICAL PROPERTY.	OUTPUT	TYPE	ABT	ALB	ВСТ	LVT	ALS	AS	1E	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHE
Octob		'543	~		V	~			V												+	
	00.08	'544					15														+	
	3S	'646	V		V	V	V	V		V								V	V		+	
Noninverting Octal Registered		'647					1			V												
riogistorou	90	'652	V		V	V	V	V		V								V	V		+	
	00/00	'653	19		84		V		8	1								- 14	2			
	OC/3S	'654	1				V															
Inverting Octal	38	'648					V	V		~												
Registered	35	'651	V				V	V		1												
		'16470	V				1		16					V								
Noninverting 16 Bit	38	'16543	V			V	1						4	V			V				+	
Registered	33	'16646	V			V	0,	-6		N			V	V				- 00	10		+	
		'16652	V			V				3			V	V			+				+	
	38	'16544								100				V								
Inverting 16 Bit Registered	3S	'16648	0		-									V								
Tiogistorou		'16651					10.							V								

OC = Open Collector OD = Open Drain 3S = 3-State



[✓] Product available in technology indicated

[•] Product available in reduced-noise advanced CMOS (11000 series)

^{*} Product available as a military device only * Product planned as a military device

⁺ New product planned in technology indicated

Bus Transceivers With Registers (continued)

DECODIDATION	OUTDUT	TVDE										TEC	HNOLO	GY								
DESCRIPTION	OUTPUT	TYPE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
30 = Open Collector Ol	Die Open Drei	'16474	HITE											V								
Noninverting 18 Bit Registered	3S	'16524	1 1/2											15			~					
Tiogistorou		'16525		H	- A		1										V					
Noninverting 18 Bit Registered With Series Resistors	38	'162525			^		-										V					
Noninverting 36 Bit Registered	3S	'32543	V																			

Bus Transceivers With Latches

DECODIDATION	OUTDUT	TVDE										TEC	HNOLO	GY								
DESCRIPTION	OUTPUT	TYPE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
Noninverting Octal Registered	3S	2952	~			~															+	
Inverting Octal Registered	3S	2953	J.HCZ1	8	~	32	188	122 U												it.		20 10
Noninverting 16 Bit Registered	38	'16952	~			~	.168	101	- 1					V			+			h,	+	

OC = Open Collector OD = Open Drain 3S = 3-State

✓ Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

+ New product planned in technology indicated

* Product available as a military device only * Product planne

* Product planned as a military device

BUFFERS/DRIVERS AND BUS TRANSCEIVERS

Universal Bus Transceivers (UBT™)/Universal Bus Exchangers (UBE™)

DESCRIPTION	OUTDIT	TVDE				TECHNOLOGY			
DESCRIPTION	OUTPUT	TYPE	ABT	ВСТ	LVT	LV	LVC	ALVC	OTHER
Noninverting 9-Bit 4-Port UBE™	3S	'16409						V	
Noninverting 9-Bit 4-Port UBE™ With Series Resistors	3S	'162409						~	
16-Bit Universal Bus Drivers	3S	'16334						+	
		'16500	V		~			~	
No. in a 40 Dis LIDTIN	00	'16501	V		~			V	
Noninverting 18-Bit UBT™	3S	'16600	V					V	
		'16601						V	
Noninverting 36-Bit UBT™	3S	'32501	V						
Noninverting 16-Bit Tri-Port UBE™	3S	'32316	V						
Noninverting 18-Bit Tri-Port UBE™	3S	'32318	V	lood) a contra	harve control of ficine and co	aconomically and	LANCO C		
OC = Open Collector OD = Open Brain 35 = 3-State	to the straight or the	'162500	~				2-00-0		
18-Bit UBT™ With Series Resistors on B Port	38	'162501	V						
Novimethig 18 Bit 38, 11962 w		'162601	V		130		4	V	
Noninverting 18-Bit UBT™ With Parity Generators/Checkers	3S	'16901						V	
20-Bit Universal Bus Drivers	3S	'16836						+	

Parity Transceivers

DESCRIPTION	OUTDUT	TVDE										TEC	HNOLO	GY							
	OUTPUT	TYPE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	НС	HCT LV LVC OTH	OTHER	
Octal	00	'656												~							
	3S	'657	V																		
8-Bit to 9-Bit Bus	38	'833	V																		
Section and an 16 Section	3S	'853	V																		
8/9 Bit	22	'29833					V								1		Ps.				
With Parity Checkers/ Generators	3S/OC	'29834			V																
		'29854			V												Pop.				
16 Bit	3S	'16657	V											V			100				

OC = Open Collector OD = Open Drain 3S = 3-State

tue Transcolvers With Hagisters (confined)

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

[★] Product available as a military device only * Product planned as a military device

⁺ New product planned in technology indicated

DECODIPTION	OUTDUT	TVDE	TECHNOLOGY																				
DESCRIPTION	OUTPUT	TYPE	ABT	ALB	ВСТ	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER	
Dual 8-Bit to 9-Bit Bus	3S	'16833	V				24							V									
Dual o-Dit to 5-Dit bus	33	'16853	1																				
Non-TTL Transce	eivers																						
TUNGERUĞ		DECODIO	TION			D ₁	04					TECHNOLOGY											
		DESCRIP						OUTPU		TYPE		ABT		BCT	L	.VT	LV		LVC	AL	/C	OTHER	
7 Bit TTL/BTL		534	Phil			1/4			OC	2041		- 5						-				√ FB	
8 Bit TTL/BTL									OC	2040												√ FB	
8 Bit TTL/BTL Registered	j	diction 1	100					100	OC	'2033									7			√ FB	
9 Bit TTL/BTL Competition	n	DVW .				Die .	40.		OC	'2032												+FB	
9 Bit TTL/BTL Address/Data								OC	2031												✓ FB		
11 Bit Incident Wave Swit	tching								OC	'1624	6			-						-		✓ ABTE	
Noninverting 16 Bit							OC	'1624	5									-		✓ ABTE			
17 Bit TTL/BTL Universal	Storage	224		-0-					OC	'1651											-	✓ FB	
Noninverting 17-Bit UBT	™ With Buffer	ed Clock O	utputs a	nd Outp	ut Edge (Control ((OECTM)		OD	'1661	6									- 19		✓ GTL	
18 Bit TTL/BTL Universal	Storage	378							OC	'1650		-										✓ FB	
18 Bit LVTTL-to-GTL/GTI	+ Registered	107						-	OC	'1692	2							7		33		+GTL	
10 Dit EVTTE-to-GTE/GT	L+ Negisteret	678							00		3											+GTL	
Noninverting 18-Bit UBT	™ With Outpu	t Edge Con	ntrol (OE	Стм)					OD	'1661	2	-										✓ GTL	
Noninverting 18-Bit UBT	М	33.0	**						OD	'1662	2											+GTL	
OC = Open Collector Ol ✓ Product available in tec ★ Product available as a	hnology indic	ated	Produc		ole in red I as a mi			nced (CMOS (1100	00 series	s)	+ New	produc	t planne	d in tecl	nnology ir	ndicated						

TEXAS

FLIP-FLOPS AND LATCHES

Flip-Flops

DESCRIPTION	OUTPUT	TYPE									Т	ECHNOI	LOGY										
	301131		ABT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER		
20	3S	73							~														
Dual J-K	00	'107			101 =0				~														
Edge Triggered		'109				V	~	V	~								~						
		'112				~		~	~	~							~			~	+CDC		
Dual D-Type		74				~	~	V	~	~	~	V.	V.	~	V		V	~	~	~			
Dual 4 Bit D-Type Edge Triggered	3S	'876	Produ	a planei	g 00 8 U	~	~																
Quad D-Type	A CHARGODA EM	'175	te Stock	of evering	Na in 18	V	V	1	V	V	1	Je sous Day	dud nis	Mest Ja J	CUEUICO	indicates	V						
Quad D-Type With Clock Enable	Lin	379							v	1,1000											cır		
Quad J-K	SLIKANSE OFF	276	s-dred (C)	(Scient)					OB	11681	V								-		NOLL		
	ATL: Regulos	'376							00	. 4605	V										GU		
Hex D-Type		'174				V	V	V	V	V							V		V		Call		
	A Sharana	'378							*	11800					10 Circ				-		10.00		
Octal D-Type True Data	00	'374	V	V	nd Edmo	V	~	V	V	V		V.	Vo	V	V		V	~	V	V	NG-SA		
	35	'574	~	*	~	~	~	V	Ole	14555		V	~	V	~		~	~	V	V	1000		
Octal D-Type True Data		'273	~		~	~			V	11694			-				V	~	V	-	STANCE.		
	3S	'575				V	V		00	HOST			-								1.10		
With Clear		'874				~	V		00	CONS											del Di		
Octal D-Type True Data With Clock Enable		'377	~					V	~	2040							~	~			Aude Aude		
7 BRITINGIL		'534	V			V			00	5041		V	V				V				FB		
Octal D-Type Inverting	3S	'564	L TUNK			V			1015.00	5.26		V	V		TAL	TA.		TAC	I VI	AC .	OUNEN		
inverting		'576				V	V									Lichio	OGA						
Octal Dual Ranked True Data	3S	'4374					V																
Octal Inverting With Clear	3S	'577	-			~										-							
Octal True Data	3S	'825	1. 15.				V																

OC = Open Collector OD = Open Drain 3S = 3-State

[✔] Product available in technology indicated Product available in reduced-noise advanced CMOS (11000 series)

[★] Product available as a military device only * Product planned as a military device

⁺ New product planned in technology indicated

Flip-Flops (continued)

DESCRIPTION

9 Bit True Data

10 Bit Noninverting

10 Bit True Data

10 Bit

OUTPUT

35

3S

35

TYPE

'823

'29823

'16820

29821

'821

ABT

V

V

BCT

V

V

LVT

ALS

*

V

AS

V

V

F

LS

S

TTL

TECHNOLOGY

ACT

AC

AHC

AHCT

ALVC

V

V

V

V

V

V

V

+

HC

HCT

LV

LVC

+

V

V

OTHER

1
Z
n
-
0
Z
D
-
Z
0
4
×

FLIP-FLOPS AND LATCHES

Latches

DESCRIPTION	NO. OF	OUTPUT	TYPE										TECHN	OLOGY								
DESCRIPTION	BITS	OUIPUI	TIPE	ABT	ВСТ	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	нст	LV	LVC	OTHER
D-Type Edge Triggered Inverting and Noninverting	8	38	'996				V															
	8	38	'990				V															
D-Type Transparent Readback, True	9	3S	'992				V															
neadback, The	10	3S	'994				V	9:							NA THE							
D-Type Transparent With Clear, True Outputs	8	3S	'666	ncy bisso	ed as a	unger k	V SANCE	,														
D-Type Transparent With Clear, Inverting Outputs	8	38	'667	hei did	inge u	equoq	~	Misson	cinos	11600	eulez)	+ 1	par proc	lac) plan	red in to	(Sojem,s	judjeraci					
Valla Senes-Demorry	- 00		'373	V	V	-	V	V	V	V	V		V.	V.	V*	V*		V	V	V	V	
D-Type	8	3S	'2373	~	1				V													
Transparent True	98	1995	'573	V	*	V	V	V	V				V	V	V*	V*	24	V	~	V	V	
	16	3S	'16373	V		V							V	V			V				~	
D-Type Dual 4 Bit Transparent True	8	38	'873				~	~														
18. 38. Mondity orders	38	JSASS	'533	V			V	V	, ,				V	V			79					
D-Type Transparent Inverting	8	38	'563		+		V						V	~				~				
Transparent inverting	0.00	1001	'580			-	V				-								-			
Addressable	8	2S	'259				V			V								V			-	
Willy Dual Oceputs	8	3S	'845				V										h. I		1			
	0	3S	'843	V			V														+	
	9	35	'29843	E,	V	1 3,															,	
D-Type True Inputs	10	3S	'841	V			1														V	
	10	35	'29841		V		V										D ₁					
	18	3S	'16843	4		*											+					
	20	3S	'16841	V			1 8							V			~				+	

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 Product available in reduced-noise advanced CMOS (11000 series) + New product planned in technology indicated



[✔] Product available in technology indicated

^{*} Product available as a military device only * Product planned as a military device

Latches (continued)

DESCRIPTION	NO.	OUTPUT	TYPE										TECHN	OLOGY								
DESCRIPTION	OF BITS	OUIPUI	TYPE	ABT	ВСТ	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	НС	нст	LV	LVC	OTHER
D-Type True Inputs With Series Resistors	20	3S	'162841	+										+								
D-Type Inverting Inputs	10	3S	'842				~															
D-Type	4		75							V												
Quad Set/Reset	ugasi	gempe outh	'279	by bysuic	iqms	raffary.	erios			V		*										
Bistable	4	n programping	'375	el cal	Male In a	4444	Lips III	The same of	NAME.	V	mios)	7.6	en Listrat	S4.07202	inchian isa	ENERGINA	ar don't last					
4 × 4 Register File			'670	-		1000a				V					-							
Dual 16 Word × 4 Bits	dyexe	3S	'870			/633	V		8													
D-Type With Series Resistors	16	3S	'162373			+			N													

BUS-TERMINATION ARRAYS

Bus-Termination Arrays

DESCRIPTION	TYPE			TECHN	OLOGY		
DESCRIPTION	TIPE	ALS	AS	F	S	TTL	ACT
10 Bit	'1071	1000					~
16 Bit	'1073	100.00					~
8 Bit Schottky Barrier Diode	'1050	5200			V		
o bit schotiky barrier blode	'1056	8075		~	~		
12 Bit Schottky Barrier Diode	'1051	150%	-		~		
President and Control of Section 1	'1016	1808		~			
16 Bit Schottky Barrier Diode	'1052	19045			~		
Dual 4-SIF Bus Suitches WRb 744 PC	'1053	4334			V		
18 Bit Schottky Barrier Diode R-C	'1018	10400		V	V		

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[✓] Product available in technology indicated★ Product available as a military device only

Product available in reduced-noise advanced CMOS (11000 series)
 Product planned as a military device

⁺ New product planned in technology indicated

BUS SWITCHES

	DEC	CRIPTION				TYPI	001/0							TE	CHNO	.OGY					
		CRIPTION				LIP	noise in	Named	CBT	(11600 s		A-M	CBTS	aci paan	Ded in te		CBTD		0	THER	
Overal Prop Cuitabas		Are l'unin	20 - 2 DH			'3125			V	-											
Quad Bus Switches						'3126			V						-						
Dual 4-Bit Bus Switche	es With '24	44 Pinout	100			'3244			V					-	-						
3-Bit Bus Switches Wit	h '245 Pir	nout	100			'3245			V	-			-								
Dual 4-Bit-to-1-Bit FET	Multiplex	ers/Demulti	iplexers			'3253			V							-		-			
8-Bit-to-1-Bit Multiplexe	ers/Data S	Selectors	121			'3251			~				-					-			
Quad 2-to-1-Bit FET M	lultiplexer	s/Demultiple	exers			'3257			V	-			-						 -		
Oual Bus Switches		Alf				'3306			~				V				~			- 6	
3-Bit Bus Switches		1949	13.0			'3345			~												-
0-Bit Bus-Exchange S	Switches	160				'3383			~	-								2.17		Lors 2	- minute
0-Bit Bus Switches	IOH	1.	AbE -	- Y	16	'3384		40	V			6.00	V		-		~	day.		44.00	سابين
0-Bit Bus-Exchange S	Switches \	With Extend	led Voltage	Range		'3386			+				CHE DAY	WUN.							
0 Bit With Precharged	d Outputs	for Live Inse	ertion			'6800			V												
8-Bit Bus-Exchange S	Switches					'16209)		V												
						'16211	NAME OF TAXABLE PARTY.	N-1. (ST)	V	PECS SC	164 30	MMTH	A.26								
4-Bit Bus-Exchange S	Switches					'16212	2		V												
						'16213	3		V									-			
2-Bit 3-to-1 Bus Selec	ct in	012	11625373			'16214			~												
Synchronous 16-Bit-to-	-32-Bit FE	T Multiplex	ers			'16232	2		V												
16-Bit-to-32-Bit FET M	ultiplexers	s/Demultiple	exers			'16233	3		V												
6-Bit Bus Switches	-		24.0			'16244			V								-				
OC = Open Collector Product available in to Product available as	technolog	y indicated	• Prod	uct avail uct plann				lvanced	CMOS	(11000 so	eries)	+ Ne	ew produ	uct plani	ned in te	chnology	indicated				



DESCRIPTION	PARALLEL	TYPE	id-rigina d	uhansed C				TE	CHNOLO	GY					
DESCRIPTION	LOAD	ITPE	ABT	ВСТ	LVT	ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	HCT
4 Bit Decade Up/Down	Sync	'568	88			~			- 2						
	- 9	'161	01			~	V	~	V					V	1
4 Bit Binary	Sync	'163	2			~	V	~	V	V	*			V	
		'561	85			~			- 2				1 1		
Swial in Paralel Out	8	'93	07						~		-				1 "
		'169	89			V	V	V	~	V	7				
4 Bit Binary Up/Down	Sync	'569	15.05 15.05			V									
		'191	00			~		I. S.	~	-	*			V	
	1 4	'193	01			V	1		~	1	~			V	1
Octal Social In With Owner Sterr on Report	Sync	'697	69						V						
8 Bit Up/Down	Sync Clear	'869	68			~	V		Phy.						1 3
	Async Clear	'867	trace L	ABT	OL T	V	V	l b	18	8 1	741.	HG W	21 163	HGL	1 0

Asynchronous Counters (Ripple Clock) – Negative Edge Triggered

DESCRIPTION	PARALLEL	TVDE						TE	CHNOLO	GY					
DESCRIPTION	LOAD	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	HCT
Dual 4 Pit Pinen	None	'390							~						
Dual 4 Bit Binary	None	'393							V		*			~	
12 Bit Binary	Async	'4040							66					~	
14 Bit Binary	794 379	'4020							Day 1					~	
14 bit binary	Async	'4060							N .					V	

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✔ Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

* Product available as a military device only

+ New product planned in technology indicated

FUNCTIONAL INDEX

* Product planned as a military device

Other Counters

DESCRIPTION	OUTDUT	TVDE						Т	ECHNOLO	GY					
DESCRIPTION	OUTPUT	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	НСТ
4 Bit Up/Down	3S	'669						644	V						
Binary With Input Register	3S	'592							V						
Decade	38	'90	nikaury des	CB	n outpoor (loss become	V		*				
Divide By 12	3S	'92	The state of		A CHICA	EURO			V		*				
16 Bit Programmable	3S	'294							V			1			
31 Bit Programmable	38	292							V						
Parallel Register Outputs	38	'590							V					V	
Parallel Register Inputs	3S	'593							V		1 4			1	

SHIFT REGISTERS

Shift Registers

TEXAS INSTRUMENTS

DESCRIPTION	NO. OF	OUTDUT	TVDE							TECHN	OLOGY						
DESCRIPTION	BITS	OUTPUT	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	TTL	AHC	AHCT	HC	HCT	LV
Octal Storage Registers	8	1838	'396					M _i		V	1						
Octal Serial In With Output Storage Registers	8	1887	'596							V							
	4	1198	'194				E. a	V		V	~	8/4					
Parallel In, Parallel Out, Bidirectional	0	1,134	'299				V		V	V	V	4					
4 Bit Bittery Up/Down	8	1999	'323				V			V							
Parallel In, Parallel Out	4	.H60	'195					-	-	V	V	*					
Serial In, Parallel Out	8	138	'164				V			V		*			V		~
Parallel In, Serial Out	0	1384	'165				V			V					V		
Faraller III, Serial Out	8	1163	'166				V	3	-54	V	-	*			V		
Social In Parallal Out With Input Latahaa	8	481	'597					=	20/	V							
Serial In, Parallel Out With Input Latches	8	1.682	'598		1		4			V	1						

OC = Open Collector OD = Open Drain 3S = 3-State

[✔] Product available in technology indicated

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

^{*} Product available as a military device only

^{*} Product planned as a military device

Shift Registers (continued)

DESCRIPTION	NO. OF	OUTDUT	TVDE							TECHN	OLOGY						
DESCRIPTION	BITS	OUTPUT	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	ΠL	AHC	AHCT	HC	HCT	LV
F Product available as a milliory device only	0	38	'594							~					~		
Serial In, Parallel Out With Output Latches	Product av	35	'595	RIVIUS	CHOS	11000 86	(GP)	+ 1/18%	mount p	~	BUJ LOPER	i izgotal	9		~		
	8		'599							V							
Nonimorting	8	3S	'299		0/4		V		V	V	V		0				
Noninverting	9	3S	'29823		10%	V	*										
16 Bit Serial In With Output Storage Registers	16	28	'673	1.3	10					V	7		3	64	2		
16 Bit Serial Out	16	St. I	'674		1 %		1 %			V							

ENCODERS, DATA SELECTORS/MULTIPLEXERS, AND BUS EXCHANGERS

Encoders, Data Selectors/Multiplexers, and Bus Exchangers

DESCRIPTION	OUTDUT	TYPE	DEN								TECH	NOLOG	Y							
DESCRIPTION	OUTPUT	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC
Data Selectors/Multiplexers		'150			in the same of						~									and a
22-to 15 VI Pag Malliferies		'157				V	V	V	V	V	V		3	+	+		~	V		~
		'158				~	~	V	V	V				+	+	-				+
Quad 2-to-1		'298					V		V		*									
Godd 2-to-1		'257			-	V	V	V	V	V				+	+		V	V		V
	3S	'258				V	V	V	V	*				+	+	+				+
Quad 2-Input Multiplexers	00	'399					ži.	-	V											
Hex 2-to-1	3S	'857				V							-			-4-				
		'153				V	V	V	V	V	*					4	V			
Dual 4-to-1	88	'253				V	V	V	V	-				-		1	V			
	3S	'353					V									- 6.				
4-to-1 Registered Transceivers	3S	'16460	V						-											-
Cascadable Octals	50	'148	1						V		V						V			
Rto.1		'151				V	V	V	V	V						6	V			
8-to-1	3S	'251	1200.1	1674	751	V	100	V	V	V	*	Tun-	W/P3	war	Strain)	yese	V	WOL	T'A	F80
8-to-3 Line Encoders	OUTPUT	'348							V		120000	Lanne						-		

OC = Open Collector OD = Open Drain 3S = 3-State

TEXAS INSTRUMENTS

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

[★] Product available as a military device only
* Product planned as a military device

TEXAS INSTRUMENTS

ENCODERS, DATA SELECTORS/MULTIPLEXERS, AND BUS EXCHANGERS

Encoders, Data Selectors/Multiplexers, and Bus Exchangers (continued)

DESCRIPTION	OUTDUT	TVDE									TECH	NOLOG	Y							
DESCRIPTION	OUTPUT	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	НСТ	LV	LVC
9-Bit 4-Port Universal Bus Exchangers		'16409				-	6.		1							V				
12-to-24 Multiplexed	3S	'16260	V				-		P.		100					V	66			
12-to-24 Registered Bus Exchangers	38	'16269	0.													V				
12-to-24 Registered bus exchangers	35	'16270					0.									V				
12-to-24 Multiplexed Bus Exchangers	38	'16271				16.	100	-	14,							+				
12-10-24 Muliupiexed Bus Exchangers	33	'16272				6	5,	1	Ps.	Th.	1					+	-			
12-to-24 SDRAM Interleave Multiplexers	52	'16268				1				F-A-						+				
16-to-1	3S	250					V		10											
16-to-32 Bit Registered Bus Exchangers With Series Resistors	33	'162280				100	Ps.	100	0,	21				-	+	+				4
18-to-32 Bit Registered Bus Exchangers		'16282												-		V				
18-to-32 Bit Registered Bus Exchangers With Series Resistors		'162282				6,	P _k	1	1	0,				+	+	+				
32-to-16 VL Bus Multiplexers		'16254				100	- 5	150		1 5/			V	+	7			100		12

DECODERS/DEMULTIPLEXERS AND OSCILLATORS

Decoders/Demultiplexers

DESCRIPTION	OUTDUT	TVDE	F BUILT							TECH	INOLOG	Y						
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	нст	LV	LVC	OTHER
Dual 0 to 4		'139	V			V	V			•	+	+		V	~		+	
Dual 2-to-4	OC	'156	V			V		V			- 7							
3-to-8	dependent 16	'138	V	V	V	V	V				+	+		V	V	V	~	
3-to-8 With Address Registers	9	'137	V	V		V	75	18									+	
4-to-10 BCD-to-Decimal	1	'42	1,0400			V		-54		-	100	1 2		V				

OC = Open Collector OD = Open Drain 3S = 3-State

[✓] Product available in technology indicated * Product available as a military device only

Product available in reduced-noise advanced CMOS (11000 series)

^{*} Product planned as a military device

⁺ New product planned in technology indicated

Oscillators

DESCRIPTION	OUTDUT	TVDE					TECHN	IOLOGY				
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	ΠL	AC	ACT	HC	HCT
		'124					V					
# Product available as a minury device only	00	'624	CHICARY GRAND			~	in the same of the					
Voltage Controlled	2\$	'628		- Participal Cit	DE WILLDOW	~		1000				
	452	'629			1 6	~			1	1		1
Crystal Controlled	28	'321			1 4	V						

COMPARATORS AND PARITY GENERATORS/CHECKERS

Comparators

achoolable			DESCRI	PTION				TVDE				TI	ECHNOLO	GY			
INPUT	P=Q	P=Q	P>Q	P>Q	P <q< th=""><th>OUTPUT</th><th>ENABLE</th><th>TYPE</th><th>ALS</th><th>AS</th><th>F</th><th>LS</th><th>S</th><th>AC</th><th>ACT</th><th>HC</th><th>нст</th></q<>	OUTPUT	ENABLE	TYPE	ALS	AS	F	LS	S	AC	ACT	HC	нст
4 Bit Binary	No	Yes	No	No	No	28	Yes	'85				V	V				
8 Bit With	No	Yes	No	No	No	28	Yes	'520	~								
20-kΩ Pullup	No	Yes	No	Yes	No	28	No	'682		1 %		V				~	
	No	Yes	No	No	No	2S	Yes	'521	~	TH.	VIII	I IK	4	ic	ACT	18	TAC
8 Bit Standard	No	Yes	No	Yes	No	28	No	'684		LEC	HOLOGY	V				~	
o bit Standard	No	Yes	No	No	No	28	Yes	'686				~					
	No	Yes	No	No	No	28	Yes	'688	~			~				~	
8 Bit Latched P	No	No	Yes	No	Yes	28	Yes	'885		V							

Parity Generators/Checkers

DECORIDATION	NO. OF	TVDE	//S		1. 13	3	TECHN	IOLOGY	CL Y	C ACT		
DESCRIPTION	BITS	TYPE	ALS	AS	F	LS	S	ΠL	AC	ACT	HC	НСТ
Odding and Podic nulls	0	'280	~	V	~	~	~					
Odd/Even	9	'286		V						•		

OC = Open Collector OD = Open Drain 3S = 3-State

✓ Product available in technology indicated

★ Product available as a military device only

* Product

Product available in reduced-noise advanced CMOS (11000 series)
 Product planned as a military device

+ New product planned in technology indicated

FUNCTIONAL INDEX

ARITHMETIC CIRCUITS

Adders

DESCRIPTION	TYPE						TECHN	OLOGY					
A DESCRIPTION	TIPE	ALS	AS	F	LS	S	TTL	НС	HCT	AC	ACT	LV	LVC
4 Bit	'283	lable in reci-	ped-noise ed	1	-	V	less product	plasmed in te	stimology inc	page 1			

Arithmetic Logic Units

DESCRIPTION	TVDE	ILE .					TECHN	OLOGY					
DESCRIPTION	TYPE	ALS	AS	F	LS	S	TTL	НС	HCT	AC	ACT	LV	LVC
Partiy Generalors/Checkers	'181		V		*	*							
4 Bit	'381					V							
	'382				V							-	

Dividers/Multipliers

DESCRIPTION	TVDE						TECHN	OLOGY					
DESCRIPTION	TYPE	ALS	AS	F	LS	S	TTL	НС	НСТ	AC	ACT	LV	LVC
Binary Rate Multipliers	'97	Mo	25	No	1,085		~		N			9.	
Digital Phase Lock Loop	'297	1/10	26	1/68	V	-							

Monostable Multivibrators

DESCRIPTION	TVDE						TECH	OLOGY				-	
DESCRIPTION	TYPE	ALS	AS	F	LS	S	TTL	НС	нст	AC	ACT	LV	LVC
1 Shot	'121						~				2. V		
1-Shot Multivibrators	'122	by M.F.	OPE A	NU DVI	~	Plast V.	WHAT	MECK!	44.5				
Duel	'123				~								
Dual Courses	'221				~	24	1						
Retriggerable	'423	9			~	2.							

OC = Open Collector OD = Open Drain 3S = 3-State

[✓] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)
 New product planned in technology indicated

^{*} Product available as a military device only

^{*} Product planned as a military device

Positive-AND Gates

DESCRIPTION	OUTDUT	TVDE							TECHN	IOLOGY						
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC
Single 2 Input		'1G08									V	~				
Oved 0 leaves	OC	'09	V			~	~									
Quad 2 Input		'7001											~			
Dual 4 Input		'21	V	~	V	~							V			
Triple 3 Input		'11	V	~	V	~	~		~	~			V			
A Libertal statement as a ungal A c	svice only " F	'08	1	~	V	~	~		V.	V.	V*	~	V	~	~	V
Quad 2 Input	project of a de-	'1008	MANUAL IN THE	~	BUTABLE	CHOS V	Offil norma	1 7 91	Mary Mariners and	Déposition (les	Incerdion	monand				
Hay O Innut		'808'		~									- 6			
Hex 2 Input		'1808		~			-								HI WAR	

Positive-NAND Gates

DECODIFTION	OUTDUT	TVDE							TECHN	OLOGY						
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC
Single 2 Input		'1G00									~	~				
8 Input		'30	~	~	~	~	~	~	n=r-re-re-re-							
13 Input	CONTROL	'133	~	149		16	V	3.63	420	Whel.	1770-	V Filed	Piter	PROJ.	TA	1 2254
Dual 4 Input		'20	~	~	~	~	~		12.1481	IN UUA			~			
Triple 3 Input		'10	~	~	~	~	~		~	~			~			~
		'00	~	V	~	~	~	~	V.	V*	V*	~	~	~	~	~
	OC	'01				~										
	3S	'26	Da.	-		~										
Quad 2 Input	93	'37	~			~	V	V				-	- 8			
	OC	'38	~	-	V	~	~	~								
		'132		-	04.	~	V	~	D ₀ 40	8.0	0.	N.	~	85.	-	1
mile z ofise		'1000		V							16					
Hex 2 Input		'804	~	V	L.	P.G.	-	- 235	360	160%	VIIIA	LOLD TO	MO	LIPSE	PA.	CAD
nex 2 input	OUTPUT	'1804		V				1	EXPANS	NEWS I						
Quad 2 Input	oc	'03	~			~	*					-	~			

OC = Open Collector OD = Open Drain 3S = 3-State

✓ Product available in technology indicated

★ Product available as a military device only

* Product

FUNCTIONAL INDEX

Product available in reduced-noise advanced CMOS (11000 series)
 Product planned as a military device

⁺ New product planned in technology indicated

Positive-OR Gates																
Checky many		100					-		TECHN	IOLOGY		-	-			
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	НС	НСТ	LV	LVC
Single 2 Input	a main manage	'1G32									~	V				
		'32	V	V	V	V	V	~	V.	Vo*	V	~	~	V	V	V
Quad 2 Input		'1032		V	6.	-		-								
	3S	'7032				-					-		V			
Hey O leave	90	'832	V	V												
Hex 2 Input	00	'1832		~		-										
	-	.00	- N		-		- A	1	1		8	N.	-		1	1
Positive-NOR Gates						O ₄										
Dual 4 logist		100							TECHN	IOLOGY						
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	НС	нст	LV	LVC
Single 2 Input		'1G02		71,	- 1	- 14	-1/				+	+				
Dual 5 Input		'260	// Am to the land		~		V					- 1				
Triple 3 Input	Onlight	'27	V	V	V	V	- 6	*	910	4.07	VIIIG	AMCT	V	160%	18	1.555
		'02	~	V	~	~	V	*	12740	DE CON			V	~	~	~
Quad 2 Input	OC	'33	*			~										
		'7002											V			
Hex 2 Input		'805	~	~											1	
nex 2 input		'1805		V												
OC = Open Collector OD = Open Down Product available in technology ind ★ Product available as a military devi	icated • F	State Product ava Product plan				CMOS (11	1000 series	s) + N	ew produc	t planned in	technolog	y indicated				
Triple 3 Input		41		Pi												

DECORPTON	AUTRIT	TVDE							TECHN	OLOGY						
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	НСТ	LV	LVC
Single 2 Input	or out	'1G86	NO 10 Rd	MSEA OSAI	9						+	+				
Oued 0 least	e parte	'86	~	aced-nois	V	01480	*	*	V.	V	~	~	V			V
Quad 2 Input	OC	'136				~										
XNOR Gates																
DESCRIPTION	OUTPUT	TYPE							TECHN	OLOGY						
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	HC	HCT	LV	LV
Quad 2 Input	OD	'266			*	~							V			
AND/NOR Gates																
AND/NON Gales	-	11034	1/4	1										1		-
									TECHN	OLOGY						
DESCRIPTION	OUTPUT	TYPE	41.0		-	1.0	-				1 4110	411000	110	HOT	1 111	1
	OUTPUT	4100	ALS	AS	F	LS	S	ΠL	AC	ACT	AHC	AHCT	НС	нст	LV	LV
Dual 3 Input	QC .	'51	ALS	AS	F	LS	S	TTL			AHC	AHCT	НС	нст	LV	LV
Dual 3 Input OC = Open Collector OD = Open Dra	ain 3S = 3-3	'51 State	3,			V	V	6,	AC	ACT			НС	HCT	LV	LV
Dual 3 Input	ain 3S = 3-3	'51	ilable in rec	duced-nois	e advance	V	V	6,	AC	ACT	AHC		НС	нст	LV	LV
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic	ain 3S = 3-3	'51 State Product ava	ilable in red ned as a m	duced-nois ilitary devi	e advance	V	V	6,	AC	ACT			НС	нст	LV	LV
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic	ain 3S = 3-3	'51 State Product ava 'roduct plan	ilable in rec	duced-nois	e advance	d CMOS (1	V	6,	AC	ACT			НС	нст	LV	LV
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic	ain 3S = 3-3	'51 State Product ava Product plan	ilable in red ned as a m	duced-nois ilitary devi	e advance	V	V) + N	AC	ACT			НС	нст	LV	LV
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic	ain 3S = 3-3	'51 State Product ava	ilable in red ned as a m	duced-nois ilitary devi	e advance	d CMOS (1	V	6,	AC	ACT			НС	нст	LV	LV
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic ★ Product available as a military device	ain 3S = 3-3	'51 State Product ava Product plan	ilable in red ned as a m	duced-nois ilitary devi	e advance	d CMOS (1	V) + N	AC	ACT planned in	technology	y indicated	НС	нст	LV	
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic	ain 3S = 3-5 cated • 1 se only * F	'51 State Product ava Product plan	ilable in red ned as a m	duced-nois ilitary devi	e advance	d CMOS (1	V	+ No	AC ew product	ACT	technolog	y indicated		нст		
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic ★ Product available as a military device	ain 3S = 3-3	'51 State Product ava Product plan	ilable in red ned as a m	duced-nois ilitary devi	e advance	d CMOS (1	V	+ No	AC ew product	ACT planned in	technolog	y indicated		нст		
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic ★ Product available as a military device	ain 3S = 3-5 cated • 1 se only * F	'51 State Product ava Product plan	ilable in rec ned as a m	duced-nois ilitary devi	e advance	d CMOS (1	1000 series	+ N	AC ew product	ACT planned in	technolog	y indicated	Pa	нст		
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic ★ Product available as a military device	ain 3S = 3-5 cated • 1 se only * F	'51 State Product ava Product plan	ilable in rec ned as a m	duced-nois ilitary devi	e advance	d CMOS (1	1000 series	+ N	AC ew product	planned in	technology	y indicated	Pa	нст		
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic ★ Product available as a military device	ain 3S = 3-5 cated • 1 se only * F	'51 State Product ava Product plan	ilable in rec ned as a m	duced-nois ilitary devi	e advance	d CMOS (1	1000 series	+ N	AC ew product	planned in	technolog	y indicated	Pa	НСТ		B
Dual 3 Input OC = Open Collector OD = Open Dra ✓ Product available in technology indic ★ Product available as a military device	ain 3S = 3-5 cated • 1 se only * F	'51 State Product ava Product plan	ilable in rec ned as a m	duced-nois ilitary devi	e advance	d CMOS (1	1000 series	+ N	AC ew product	planned in	technolog	y indicated	P ₁	нст		LV

TEXAS INSTRUMENTS

HEX INVERTERS/NONINVERTERS AND DELAY ELEMENTS

Hex Inverters/Noninverters

DESCRIPTION	OUTDUT	TVDE							TECHN	IOLOGY						
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	HCT	LV	LVC
		'04	V	~	V	V	V	~	V.	V.	V	~	V	~	V	V
		'U04									V		V		V	1
		'1G04								+	+					
		'1GU04								+	+					
	OC	'05	V			~	V	V					V			
Have become	00	'06				~		V								
Hex Inverters		'14				~		V	~	V*	V	~	V		~	~
		'1G14									+	+	a .			
		'16						V								
		'19				~										
		'1004	~	~												
A Committee of the Comm	land a	'1005	~	likes I contin												
 Product grafiable in lachaniegy indic 	OC	'07	SCHOOL STATE	G084-L0G	# BDASSJOSK	~	000 1949	V	w brogne	Designation of	pannon	Belacated				
	7 33 - 34	'17						~								
	OC	'35	~			24	Pog.									
Hex Noninverters	main by an at a	'128	ALS	Y8	la	1.8	8	V	y.c	VOL	Visit	THELL	HC	HOL	. 174	1060
riex Normityerters	OHODHE	'140					~		18096	DFOCA						
		'1034	~	V									a.			
	OC	'1035	~													
		'4066											~			

Delay Elements

DESCRIPTION	OUTDUT	TVDE								OLOGY						
DESCRIPTION	OUTPUT	TYPE	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	HC	НСТ	LV	LVC
Hex		'31				~										

OC = Open Collector OD = Open Drain 3S = 3-State

[✔] Product available in technology indicated

 Product available in reduced-noise advanced CMOS (11000 series)

[★] Product available as a military device only
* Product planned as a military device

⁺ New product planned in technology indicated

INSTRUMENTS

IEEE 1149.1 (JTAG) BOUNDARY-SCAN LOGIC DEVICES

IEEE 1149.1 Boundary-Scan Logic

C = Clocked	IPTION		NO. OF	AUTRUT	TVDE					TECHN	OLOGY				
DESCR	IPTION		BITS	OUTPUT	TYPE	ABT	ВСТ	LVT	F	LS	S	TTL	AC	ACT	OTHER
D. # /D-:	овисе разу	Lucottex benause	8	00	'8240		V								
Buffers/Drivers			N 189 1000	3S	'8244	1000 sema	1	lew produc	bigoned a	technolog	k jegeljer)				
OC = Open Collector OD = Ope	n Dalin 35 - 3	24	8	3S	'8245	V	~								
Transceivers			18	3S	'18245	V		+							1
Transparent Latches	n'c	85 78	8	3S	'8373		V							15	100
Flip-Flops	n	38 125	8	3S	'8374		V								
京 東京 × 京 (100)	I II	26 22	10		'8543	V						-			
					'8646	~									
			8	3S	'8652	V	9								
A1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1					'8952	V									
Registered Transceivers					'18502	V		V*			2				
			18	3S	'18646	V		+							
					'18652	V		+		0					
			20	3S	'18504	~	8	~	8	18	8	TIL T	VC	ACT	VI.NU
Inverting Bus Transceivers			18	3S	'18640				ECHHOL:	GA					
Inst-in, First-Out (FIF	O) Mamon	108			'18512			+							
LIDTM			10	00	'182512			+							
UBT™			18	3S	'18516		e solve alle	+							
					'182516	2951953	Birth .	+							
UBT™ With Series Output Resist	torsParity Genera	ators/Checkers	18	3S	'182502	V		~							
LIDTIN	- 14	one I	00	00	'18514			+					0		
UBT TM			20	3S	'182514			+					1 0		
UBT™ With Series Output Resist	torsParity Genera	ators/Checkers	20	3S	'182504	V	T V								

OC = Open Collector OD = Open Drain 3S = 3-State

✓ Product available in technology indicated • Product

Product available in reduced-noise advanced CMOS (11000 series)
 Product planned as a military device

* Product available as a military device only

+ New product planned in technology indicated

FUNCTIONAL INDEX

TEXAS INSTRUMENTS

IEEE 1149.1 (JTAG) BOUNDARY-SCAN LOGIC DEVICES

Scan-Support Devices

DESCRIPTION	TVDE					TECHN	IOLOGY				
DESCRIPTION	TYPE	ABT	BCT	LVT	F	LS	S	ΠL	AC	ACT	OTHER
Test Due Controllers	'8980			+							
Test Bus Controllers	'8990	printerio ar con	portugin cons	inea neemo (Lippo souss)	La. Mark hunor	r historian et ren	umic3), paicss	0	~	
Digital Bus Monitors	'8994									~	
Addressable Scan Port Devices	'8996	V .	33	1.85204	1 1						
Scan-Path Linkers	'8997			1.162514		1				~	
Scan-Path Selectors	'8999	- 1 - 0	- 10	18914		1 4				~	

FIFO MEMORIES

First-In, First-Out (FIFO) Memories

DESCRIPTION		OUTDUT	TVDE	1		10			TECHN	IOLOGY					
SIZE	TYPET	OUTPUT	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	ALVC
16 Words × 4 Bits	- 1	200	'224		1488	9	S			~				1	
16 Words × 4 Bits	U	3S	'232	3	1 198	8	V								
16 Words v. F. Dits	- 11	3S	'225		.128	5 1					V				
16 Words × 5 Bits		35	'233		203		~								
32 Words × 9 Bits	В	3S	'2238	1 2	1888		~		1						
64 Words × 4 Bits	U		'236		7.884		~							<u> </u>	
64 Words × 8 Bits	U	3S	'2232		185.4		~								
64 Words × 9 Bits	U	38	'2233	1 2	1937		~							1	
CAllerda . 40 Pia	U, C	3S	'7813	3	1.9333									V	V
64 Words × 18 Bits	U	3S	'7814	3	1.495			- 2						V	V

OC = Open Collector OD = Open Drain 3S = 3-State

- B = Bidirectional
- C = Clocked
- S = Synchronized

 [✓] Product available in technology indicated
 ★ Product available as a military device only

[•] Product available in reduced-noise advanced CMOS (11000 series)

⁺ New product planned in technology indicated

^{*} Product planned as a military device

[†]U = Unidirectional

DESCRIPTION									TECHN	OLOGY					
SIZE	TYPET	OUTPUT	TYPE	ABT	ВСТ	LVT	ALS	AS	F	LS	S	ΠL	AC	ACT	ALV
	20		'3612	~											
0.1111 1 00.00	B, C	3S	'3614	~											
64 Words × 36 Bits			'3611	V											
	U, C	3S	'3613	~											
D 101 1			2226											V	
Dual 64 × 1	C	3S	'2227											V	
D 1050 4			'2228											V	
Dual 256 × 1	С	3S	'2229											V	
256 Words × 9 Bits	U	3S	'7200L											~	
050.14	U, C	3S	'7805											~	V
256 Words × 18 Bits	U	3S	7806											~	~
256 × 36 × 2 Bits	B, C	38	'3622											~	
540 W	gavios pur).	00	'7201LA	res), esevice										~	
512 Words × 9 Bits	U	3S	72211L	cod-naise s	dyanesá C	108 (H1000	26fl08)	4-New po	duct plann	ed in techno	ngy indeal	iq pi		~	
DC = Open Collector - OD = Op	U, C	38	'7803											V	~
540 Wests - 40 Pts	Ü	3S	'7804											V	V
512 Words × 18 Bits	B, C	3S	7819	~										- 4	
	В	3S	'7820	~										- %	
512 Words × 32 Bits	B, C	3S	'3638											V	
540 W 1 - 00 P2-	U, C	38	'3631											V	
512 Words × 36 Bits	B, C	3S	'3632											V*	
SK Mords × 8 Dan	В	38	'2235											V	
1K Words × 9 Bits		00	'7202LA											V	
	U.	3S	72221L											~	
1K Words × 9 Bits × 2	В	38	'2236											V	
OC = Open Collector OD = Op			7802											8	1
Product available in technolog			ailable in redu			MOS (11000) series)	+ New pro	oduct plann	ed in techno	ology indicat	ed			
★ Product available as a military U = Unidirectional	device only	Product plan	nned as a mili	nary device											
B = Bidirectional															
C = Clocked	LABEL														
S = Synchronized															

First-In, First-Out (FIFO) Memories (continued)

FIFO MEMORIES

First-In, First-Out (FIFO) Memories (continued)

DESCRIPTION									TECHN	OLOGY					
SIZE	TYPET	OUTPUT	TYPE	ABT	BCT	LVT	ALS	AS	F	LS	S	ΠL	AC	ACT	ALVO
U = Unicitégiores B = Ridentimal	11.0	-00	'7811											V	
	U, C	3S	'7881	mal pauce										V	
1K Words × 18 Bits	The state of the s	Productiens	'7801	keq-uopsis	dvanced C	HOS (1100)	eeujou)	-j- (40% ba	agino; bisus	ed in lection	offix proposi	ig .		V	
	U U	3S	7802											V	
1K Words × 36 Bits	U, C	3S	'3641											V	
	U, C	3S	'7807	150										~	
1K Words × 9 Blas			'7203L											V	
2K Words × 9 Bits	U	3S	'7808											V	
	B, C	35	'72231L											~	
2K Words × 18 Bits	С	3S	'7882											V	
612 Wheek × 30 BHs	8.0	38	'7204L											~	
4K Words × 9 Bits	U	3S	'72241L	- 5										~	
8K Words × 9 Bits	U	3S	'7205L	Pi										~	
	_													- 2	14.
16K Words × 9 Bits OC = Open Collector OD = Open Dr ✓ Product available in technology indi	rain 3S = 3-	3S State Product ava	'7206L ailable in redu	uced-noise a	dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed		2	100
OC = Open Collector OD = Open Dr Product available in technology indi Product available as a military device U = Unidirectional	rain 3S = 3- licated • ce only *	State Product ava Product plan	ailable in redu nned as a mil		dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed		0.	1,
OC = Open Collector OD = Open Dr Product available in technology ind Product available as a military device U = Unidirectional B = Bidirectional	rain 3S = 3- licated • ce only *	State Product ava Product plan	ailable in redu nned as a mil		dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	blogy indicat	ed		100	14
OC = Open Collector OD = Open Dr Product available in technology indi Product available as a military device U = Unidirectional	rain 3S = 3- licated • ce only *	State Product ava Product plan	ailable in redu nned as a mil		dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			N.
OC = Open Collector OD = Open Dr Product available in technology ind Product available as a military device U = Unidirectional B = Bidirectional C = Clocked	rain 3S = 3- licated • ce only *	State Product ava Product plan	ailable in redu nned as a mil		dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			
OC = Open Collector OD = Open Dr ✓ Product available in technology indi ✓ Product available as a military device U = Unidirectional B = Bidirectional C = Clocked S = Synchronized	rain 3S = 3- iicated • ce only *	State Product ava Product plan	ailable in redu ned as a mil		dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			
OC = Open Collector OD = Open Dr ✓ Product available in technology indi ✓ Product available as a military device U = Unidirectional B = Bidirectional C = Clocked S = Synchronized	rain 3S = 3-licated • ce only *	State Product ava Product plan	ailable in redu nned as a mil		dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			
OC = Open Collector OD = Open Dr ✓ Product available in technology indi ✓ Product available as a military device U = Unidirectional B = Bidirectional C = Clocked S = Synchronized	rain 3S = 3- icated • ce only *	State Product ava Product plan	ailable in redu ned as a mil		dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			- N
OC = Open Collector OD = Open Dr ✓ Product available in technology indi ✓ Product available as a military device U = Unidirectional B = Bidirectional C = Clocked S = Synchronized	rain 3S = 3- iicated • ce only *	State Product ava Product plan	ailable in redu ned as a mil		dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			
OC = Open Collector OD = Open Dr ✓ Product available in technology indi ✓ Product available as a military device U = Unidirectional B = Bidirectional C = Clocked S = Synchronized	rain 3S = 3- iicated • ce only *	State Product ava Product plan	ailable in redu ned as a mil		dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			
OC = Open Collector OD = Open Dr ✓ Product available in technology indi ✓ Product available as a military device U = Unidirectional B = Bidirectional C = Clocked S = Synchronized	rain 3S = 3- icated • ce only *	State Product ava Product plan	ailable in redu ned as a mil	itary device	dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			N. N.
OC = Open Collector OD = Open Dr ✓ Product available in technology indi ✓ Product available as a military device U = Unidirectional B = Bidirectional C = Clocked S = Synchronized	rain 3S = 3- iicated • ce only *	State Product ava Product plan	ailable in redu ned as a mil	itary device	dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			
OC = Open Collector OD = Open Dr ✓ Product available in technology indi ✓ Product available as a military device U = Unidirectional B = Bidirectional C = Clocked S = Synchronized	rain 3S = 3- iicated • ce only *	State Product ava Product plan	ailable in reduned as a mil	itary device	dvanced C	MOS (11000	series)	+ New pro	oduct planne	ed in techno	ology indicat	ed			

LOGIC OVERVIEW	1
FUNCTIONAL INDEX	2
FUNCTIONAL CROSS-REFERENCE	3
DEVICE SELECTION GUIDE	4

병에 하는 원수를 하보내다가 없어 [생태 6

SECTION 3 FUNCTIONAL CROSS-REFERENCE

section s Unctional oross-reference

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DEVICE		BiC	MOS				BIPC	DLAR							CMOS					OTHER
DEAICE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
'1G00	PAPER.	State of the state			CAN WE AV	Sehin in	DOLLARY D	Here or A.	Park Cali	IS WEST		77	V	V	Torilord's	The second	124			
'1G04													+	+						
'1GU04											-		+	+						-
'1G08						-				-			V	V		-				
'1G14	-						- "						+	+						
'1G32	100			- 1				- 14					V	V						
'1G86														+						
'00					V	V	V	V	V	V	V.	V*	V*	V		V	V	V	V	
'01								V		*										
'02					V	V	V	V	V	*			+	+		V	V	~	1	
'03					V		- 14	V	*		-									
'04					V	V	V	V	V	V	V.	V.	V	V		V	~	V	V	
'U04										- 3			~			~		V	V	-
'05					V			V	V	V						V				
'06								V		V				-						
'07								V		V										
'08					V	V	V	V	V	-	V.	V.	V*	V		V	V	V	~	-
'09					V			V	V		-			-			-			-
'10					V	V	V	V	V		V	V				V			~	
'11					V	V	V	V	V		V	V		-		V				
'14						-	- "	V	- 10	V	V	V*	V	V		V	*	V	V	
'16										V										
'17					-				-	V										
'19								V										-		
'20					V	V	V	V	V	- 3						V				-
'21					V	V	V	V								V				
'26							-	V												-
'27	-				V	V	V	V	- 3	*						V				
'30					V	V	V	V	V	V										-
'31					- 19			V												

Product available in reduced-noise advanced CMOS (11000 series)
 Product planned as a military device

⁺ New product planned in technology indicated

 [✔] Product available in technology indicated
 ★ Product available as a military device only

DEVICE		BiC	MOS				BIPO	DLAR							CMOS					OTHER
DEVICE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
'32	and a mile	A CONTRACTOR		6.75	V	V	V	V	~	1	V.	V.*	V	V		V	V	~	~	
'33					*			V		-		-								
'35					V		-0	-	0	-	-									
'37					V	- 14		V	V	V										
'38					V		V	V	V	V										
'42					-	- 1	-	V			-					V				
'45						- 24			- 3	V						- 13	-			
'47								V		V										
'51								V	~	*										
'73								V		130										
'74					V	~	V	V	V	V	V.	V.	V*	~		V	V	V	V	
'75					2%			V	2774											
'85	-					- 2	- 2	V	V											
'86					V	*	V.	V	*	*	V.	V	V	~		~		-	~	
'90					-	73		V		*	775,0									
'92							7	V		*	-									
'93								V												
'97								-		1				-						
'107								V		*			-	-			-			
'109					V	~	V	V		1	-	200				V				
'112					V		~	V	V					-		~			~	
'121							-7	- "	2.6	V				1					-	
'122								V		*	-			-					-	
'123								V	- "	V	-									
'124									V											
'125	V		V	V			V	V					V*	V*		V	~	~	V	
'126	V		V				V	~		*	-		V*	V*		V			V	
'128										V										-
'132								V	V	~						~				
'133					V				V										-	

 [✔] Product available in technology indicated
 ★ Product available as a military device only

Product available in reduced-noise advanced CMOS (11000 series)

^{*} Product planned as a military device

[→] New product planned in technology indicated



DEVICE		BiC	MOS				BIPC	OLAR							CMOS					OTHER
DEVICE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	НС	HCT	LV	LVC	UINER
136	- The Paris	,						~	1 100 21	- 1111000		7. 77								
137					V	~	1270	V											+	
138					V	~	~	1	~				+	+		V	~	V	V	
139					1			1	~				+	+		~	~		+	-
140									V											-
145							-	V	4	1										
148			-			dia .		V		V						V				
150										~										
'151					~	V	V	V	~							V				
'153					V	~	V	V	~	*						V	-			
'154										~						A.				
'155								V		*										
'156					1			~		~										
'157					~	~	V	V	~	V			+	+		V	V		V	
'158					~	~	V	V	V				+	+					+	
'159										V										
'161					~	~	V	V			-					V				
'163					V	V	V	V	V	*						V				
'164					~			V		*						V		~		
'165					~			V								V		~		ACAC
'166	-				1			V		*			0.			V				J-CAC
'169					1	V	V	V	V											11110
'173			-					V	-	*						-				
'174					V	V	V	V				0.0				V		V		
'175					V	V	V	V	V	V						V				200 LI
'181						V		*	*											000.11
'191					V			~		*						V				OCH LI
'193					V	-		V		~						~				
'194						V		V	V										-	0001.0
'195					-			V	V	*				-		*				

 [✔] Product available in technology indicated
 ★ Product available as a military device only

Product available in reduced-noise advanced CMOS (11000 series)
 * Product planned as a military device

⁺ New product planned in technology indicated

DEVICE		BiCI	MOS				BIPO	DLAR							CMOS					OTHER
DEAICE	ABT	ALB	ВСТ	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	НС	НСТ	LV	LVC	OTHER
'221			Pr d'oran			and the feet		V	7.071	*		7 (7"								
'224								V			-									See FIFO
'230	-					V										100				
'232	-				V		-									150				See FIF
'233					V						-									See FIF
'236	-				V															See FIF
'240	1		V	V	V	V	V	V	V		V.	V.	V	V		V	~	V	+	
'241	V		V	V	V	V	~	V	V		V	V				V			+	
243					V		~	V										7		
'244	V		V	V	V	V	V	V	V	-	V.	V.	V*	V		V	~	V	V	+LVCh
'245	V		V	V	V	~	V	V			Vo*	V.*	V*	V		V	V	V	V	+LVCI
247								V										in the		
'250	-					V				-										
'251					~		~	V	~	*						V				
'253					V	V	V	V								V				
'257					V	V	V	V	V			•	+	+		V	V	alangua kite bersesia	V	
'258			·		~	V	V	V					+	+		-			+	
'259					V			V	-		-					V				
'260							~		~			-	-							
'266								~								~				
'273	V			~	V			~	-		-				A	V	V	~		
'276										~										
'279								V		*										
'280					V	V	~	V	V							16.				
'283					-		V	V	V											
'286						4			-			•								-
'292								V	-								- 6		- 6	
'294					-	-		V	-	-		-					-	h		
'297				-				V	-	-										
'298						V		V		*									-	

 [✔] Product available in technology indicated
 ★ Product available as a military device only

Product available in reduced-noise advanced CMOS (11000 series)

^{*} Product planned as a military device

⁺ New product planned in technology indicated

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DEVICE		BiC	MOS				BIPO	DLAR							CMOS					OTHER
DEVICE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
'299	Bolisha Fri it		Jack Street	9.5	V	doble in	V	V	4	NG VARUE	-	de No	o trong n	ilentied i	- Sandhigalic	no inclina	-			
'321								V												
'323					V			V		-	-									
'348								V			-	-								
'353						V														
'365	-		- 13		17		- 6%	V		*						V				-
'367							- *	V		V						V				
'368	-		*					V		V						V				
'373	V		V		V	V	V	V	~		v.	10	V*	V*		V	V	V	V	
'374	V		V		V	V	V	V	~		v.	V.	V*	V*		V	V	V	V	
'375								V										Cappel St. St. Str.		
'376								-		V										
'377	V						V	V								V	V			
'378								V								-				
'379								V												
'381								13	V											
'382								V												
'390	-				-			~			-									
393								V		*						V				
'396								V			-					101				-
'399	-				-	- 7%		V												
'423					73		- 23	V					*365	- 73						
'442					-	- 10		~			-			- 164						
'465					13			V												
'466								V												
'520					V							100					E.			
'521				-	V		V				- 1					_3_				
'533	V				V	V					V	V								
'534	V				V						V	V				V				
'540	V		V		V		- 15	V					V*	V*		V	V		+	

[✔] Product available in technology indicated★ Product available as a military device only

Product available in reduced-noise advanced CMOS (11000 series)
 * Product planned as a military device

⁺ New product planned in technology indicated

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NO.	EX.
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STA	

DEVICE		BICI	MOS				BIPO	DLAR							CMOS					OTHER
DEVICE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	НС	HCT	LV	LVC	OTHER
'541	V	rdinal an	V	9 8	V	Medda in a	V	~	Cong Large	S CHANN	and as a	de Mar	V*	V*	Ind-min	V	~		+	
'543	1		V	V			V	-					1,47	- 100			-	-	+	
'544											-	-							+	
'561	-				V					-	-									
'563					V		- 1				V	V				V				
'564					V						~	V								-
'568					V			7												
'569					V			- 64												
'573	V		*	V	V	V	V				V	V	V*	V*		V	V	V	V	
'574	V		V	V	~	V	V	1			V	V	V*	V*		V	V	V	V	
'575					1	V														
'576					V	V		13												
'577					V			- 01/2						-			-			
'580					V			-				-						-		
'590								V				-				V			-	
'592								V												
'593								V										-		
'594								V								~				
'595	17							1			-	-		-		V		-		
'596								V		-		-		-				-		
'597								V										-		
'598	-		-		-		- 24	V	-		100	17.	73.5	- 70			-			-
'599	-					- 10	20	V			- Colo	100	- 14	- 3-		100	-	-	-	
'620	V		*		V													-		-
'621					V		*			1				-						-
'623	V		V		V		V	V	-							V	1			
'624						-/		V												
'628								V												
'629					-			V											-	
'638					V			-												

 [✓] Product available in technology indicated
 → Product available in reduced-noise advanced CMOS (11000 series)
 → Product available as a military device only
 → Product planned as a military device

⁺ New product planned in technology indicated

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DEVICE		BiC	MOS				BIP	OLAR							CMOS					OTHER
DEVICE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
'639	Selfa in i	Spirit S	(Unglive, un	0.70	V	V	of free factors	An order	med Chi	OR HARD	(ander)	de Ma	Classing No	Annual Control	programmy	the indicate	24			
'640	V		V		V	V		V								V				
'641					V	V		V								-				
'642	-				V	- 1		V												
'645	-				V	V		V								~	V			
'646	V		V	V	V	V		V								V	V		+	
'647								V												
'648					V	V		V												
'651	V				V	V														
'652	V		V	V	V	V		1								~	V		+	
'653					V	- 00														
'654					V	- 25														
'656																				
'657	V				-															
'666					V	-														
'667	15				V														1	
'669	1							V											7	
'670					- 1			V												
'673	-							V												
'674								V												
'682	100				- 11			V								V				
'684								V								V				
'686	-		. I de como		-2			V												
'688	10				V			V								V				
'697					100	- 100		V												
756			V			V													1 1	
757	15					V													+	
'760			V		V	V														
'804	15				V	V													1	
'805	-				V	V														

[✓] Product available in technology indicated★ Product available as a military device only

Product available in reduced-noise advanced CMOS (11000 series)
 New product planned in technology indicated
 Product planned as a military device

^{*} Product planned as a military device

DEVICE		BiCl	MOS				BIP	DLAR							CMOS					OTHER
DEAICE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
808	1910/10/20/2	Market House	in the state	4.5	Colored steel	V	the second of	July William	Mail (3)	OS INTROD		do Ma	THE REAL PROPERTY.	demedi	Lambordo	an feeting				
821	V				-	V													+	
823	V					V													+	
825			- "		-	V					-									
827	V																		+	
828			- 2			10													+	
832					V	V		13.												
833	V				- 5			- 5								- 1				
841	V				V			7%											+	
842	-				V			- 7												
843	V				V			- 1%								- 1			+	
845					V			- N												
853	V																			
857					V			79												
'861	V							-											+	
863	V				-														+	
867					V	V														
869	- 15				V	V														
870					V							-								
873					V	V														
874					V	V														
876	-		- 14	19	V	V		- 10				-					1		+	
885	-			à.	7%	V														
990					V	-		-												
992					V			100												
994	100		100	- 8%	1	- 01		15								4	-		+	
996					V	Ph.		95								77	114			
1000					1	V		100												
1004					2	V		1		1										
1004	1		0.		V	-		100												

Product available in technology indicated * Product available as a military device only

Product available in reduced-noise advanced CMOS (11000 series)

^{*} Product planned as a military device

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DEVICE	a opje sti	BiC	MOS		ponts by		BIP	OLAR							CMOS					OTHER
DEVICE	ABT	ALB	ВСТ	LVT	ALS	AS	F	LS	S	TIL	AC	ACT	AHC	AHCT	ALVC	HC	НСТ	LV	LVC	
1008						V														4-CBT
'1016							V													⇒'ÓULD.
'1018							V													L/CBT
'1032						V														PACRI
'1034					V	V														► CBTD.
'1035					V															INCRL.
'1050									V											*NCBL
'1051									V											+C8T
'1052									~										+	MCB1
'1053									~	1										*YCBT
'1056							~		V											1-08T
'1071												~								- ACBT
'1073			- 15									~								
'1244	100			Ph.	V														+	
'1245			1		V															
'1284	24		Deg :									V								
'1640					V															
'1645					V		- 0,													
'1650	I h		01				100				-								+	✓FB+
'1651																	-			V FB+
'1804						~														
'1805						V				-		-	-			-		-	-	
'1808	-					V	- Interest	100000000000000000000000000000000000000								-				
'1832						~														Government of the
'2031																				✓FB+
'2032																-				✓FB+
'2033					-															✓FB+
'2040					-															✓FB+
'2041												- 1								V FB+
'2226												V								See FIF

 [✓] Product available in technology indicated
 ★ Product available in reduced-noise advanced CMOS (11000 series)
 ★ Product available as a military device only

⁺ New product planned in technology indicated

DEVICE		BiC	MOS				BIPO	DLAR							CMOS					OTHER
DEVICE	ABT	ALB	BCT	LVT	ALS	AS	F Y	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
'2227	mids in t	chrofor	inducto.	4.0	19 AL 200	Enfelia by a	shand s	See of the co	read Chile	NO SETURBLE	services)	V	r transfirms		Econolistic Co.	at inches	19			See FIFO
'2228												V								See FIFC
'2229												~								See FIFC
'2232					V															See FIFC
'2233					V															See FIFC
'2235												V								See FIFC
'2236												V								See FIFC
'2238					V															See FIFC
'2240	V		V		1	-														
'2241	V																			
'2244	V		~				V												~	200
'2245	V		V				~												+	✓LVCR +LVTR
'2373					By		~													
'2541					V															3
'2827	V		~									Ps,								
'2828			~		100															
'2952	V			V	100														+	
'2953			~									Brog								
'3125												Di.								✓ CBT
'3126							00		14											+CBT
'3244									04											✓ CBT
'3245									25										+	✓ CBT
'3251									94											+CBT
'3253									- Pig											✓ CBT
'3257					1															✓ CBT
'3306					54	P ₁										-				✓CBT,D,
'3345						Pil														✓ CBT
'3383							Page 1													✓ CBT
'3384							Ą												-	✓CBT,D,
'3386						84														+CBT

Product available in technology indicated

^{*} Product available as a military device only

^{*} Product planned as a military device

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DEVICE		BiC	MOS				BIP	OLAR							CMOS					OTHER
DEAICE	ABT	ALB	BCT	LVT	ALS	AS	F. F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	НС	HCT	LV	LVC	OTHER
'3611	V	ruperiya.s	and other	. 0	ordinal end	Dodda in c	rived.	jou squar	CONTRACTOR	S 11 (UD)	and and	-A Mo	- Street In	deres of h	Ecolosedo.	an itrigues,				See FIF
'3612	V							-				- "								See FIF
'3613	1																			See FIF
'3614	V					-														See FIF
3622												V								See FIF
'3631								1				V								See FIF
'3632				7								V*								See FIF
'3638												V								See FIF
'3641	-											V*								See FIF
'4020	-															V	-			See 17.4
'4040	-				-											~				Son l'Ele
'4060			- 19													~				Son ITA
'4066			- "											-		V				See ITA
'4245	-		- 17																+	✓ LVC
'4374						V												-		Sec ITA
'5400	V																			S- III
'5401	V																			Saa File
'5402	V										-									S 1716
'5403	V										-									Con Etc
'6800																	-			✓ CB1
'7001												-				V				See Diff.
'7002												100				V				See DIC
'7032												100				V				679 EIE
'7200L												V								See FIF
'7201LA												V								See FIF
'7202LA											-	V			- 3					See FIF
'7203L												V			- 13					See FIF
'7204L												V			- "					See FIF
'7205L												V			-					See FIF
'7206L												V								See FIF

[★] Product available as a military device only
* Product planned as a military device

DEVICE		BiCl	MOS				BIP	DLAR			CMOS									
DEVIOL	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
'7801	Calde in	The state of the s	indicate.		200 mg 100	aren er	and record to	stea article	mared (1994	AC UNDUA	politicit.	V	T. Constant	ednoment i	Paramana and a second a second and a second	an inches	loca .			See FIF
'7802												V								See FIF
'7803												V			~					See FIF
'7804												V			~					See FIF
7805										-		V			V					See FIF
7806	-											V			V					See FIF
7807												V								See FIF
7808					-							V								See FIF
'7811			-									V				- 2				See FIF
7813					-							V			V	- 1			-	See FIF
7814												V			V		and the same			See FIF
7819	V																			See FII
7820	V																			See FII
7881												V								See FIF
7882	-75											V								See FII
'8240	+		V																	See JT
'8244	+		V																	See JT/
'8245	V		V																1	See JT/
'8373	+		V													21,				See JT/
'8374	+		V					-								0				See JT/
'8543	V															- 14				See JT
'8646	V													-		-				See JT
'8652	V											-								See JT
'8952	V																			See JT/
'8980				+								47.4								See JT
'8990												V								See JT/
'8994												V								See JT/
'8996	V																			See JT/
'8997	- 17											V								See JT/
'8999	1											V								See JT

Product available in technology indicated

^{*} Product available as a military device only

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i	\leq	A		
	Z	V	1	
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DEVICE		BiC	MOS				BIPO	DLAR			CMOS									
DEVICE	ABT	ALB	BCT	LVT	ALS	AS	. Fλ	LS	S	ΠL	AC	ACT	AHC	AHCT	ALVC	НС	нст	LV	LVC	OTHER
11000	Puble in 1	edirologi	Indicates	0-1	educt av	Parities in a	SONOSQ-U	ACC SOAR	read ONE	S (1100)	V	No	# Dischiri	Special st	herbrydo	an juganan	18			
'11004											V	~								4611
'11008											V	V								
'11032											V	V								- AGE
'11074											V	V								- MOD
'11086	3/										V				- 1					
'11138	1										V				- 5%					
'11139											V	V								
'11240	100			- 10							V	V			100				+	
'11244	10										V	V			4				-	
'11245	19										V	V			7				17/	
'11257											V	V			174,					
'11286												V			- 6/					
'11373	10%			Phy							V	V			0.0					
'11374	100			85,							V	V			. 1					
'11652											V	V								
'16209												15,								✓ CBT
'16211											16									✓ CBT
'16212	94											15								✓ CBT
'16213	1																			✓ CBT
'16214															8					✓ CBT
'16232	100			100							- 0/	2/			75				2	✓ CBT
'16233	- 75			-			3				1	354			24				- 6/	✓ CBT
'16240	V										V	V			V				V	
'16241	V											V			+				+	
'16244	V	V		V							V	V			V				V	+CBT
'16245	V	V		V							V	V			V				V	✓ ABTE
'16246	V														Ph.					✓ ABTE
'16254												V			9/4					
'16260	V														V					

 [✓] Product available in technology indicated
 ★ Product available as a military device only

Product available in reduced-noise advanced CMOS (11000 series)
 → New product planned in technology indicated
 * Product planned as a military device

DEVICE		BiCI	MOS				BIP	OLAR			CMOS									
DEVIOL	ABT	ALB	BCT	LVT	ALS	AS	ug File	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTHER
'16268	lable in t	dimology	li i glangba	0 15	polyect may	Nether II v	equipose-u	ese cqusi	ided CW	GS (11660)	saries	4. 1/19/	i creding	DANCHES &	+		M			
'16269	-														V					
'16270												100			V					
'16271	-														V					KART
16272	-	- 1		3							- 7	-			+				- 1	47ART
16282	-	- 1		- 1							-	100			V				-	408:
16334	1/4											-			+				-	
16344	- 1										- 1	- 5%			+				-04	
16373	V			V							V	V			V				V	- NUB
16374	V .			V							V	V			V				V	- WCB
'16409															V					PACE
'16460	V																			6/08
'16470	V											V								L/CS
16472											V									L/CS
16474												V								PNU8
16475											100	V								
'16500	V			V							- 1	2/4			V					
'16501	V			V							- 0/-	- 7%			V					
'16524												100			V					
16525											- 15	65			V					
16540	V										100	V			+				V	
'16541	V										-	V			+				V	
'16543	V			V							V	V			V				+	
'16544											10,	V								
'16600	V										- 00				V					
'16601	V										15				V					
16612											- 1	-0								✓ GT
'16616											1	2/								✓ GT
'16620											V	V								
16622											D ₁	100								+GT

⁺ New product planned in technology indicated AGT AHG ANGT ALVE NG NGT LY EVE



DEVICE		BiC	MOS				BIP	OLAR			CMOS									
# Product an	ABT	ALB	ВСТ	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	НС	HCT	LV	LVC	OTHER
'16623	V	The state of the s	i indicato		LAPIN DA	STAND ST	Lanca and a	7000	- arten	INS THE HOUSE		V	100000	Tallockood is	- South-order	on project				
'16640	1	-		- 1							~	~								*\$17100
'16646	V			V							V	V			19				+	-
'16648												4								
'16651												V								Soo FIF
'16652	V										1	V			+				+	Sal Fig
'16657	V											V								See Fire
'16721												256			V					Ran Flig
'16820															V					
'16821	1											V			V			-		
'16823	V										V	V			V					
'16825	1											V			V					
'16827	V											V			V					
'16830					10										+					
'16831			100												+				i de la companya de l	
16833	V		- 15									V								
'16835			- 1	V	7%										V					
'16836			814												+					
'16837					3/															+SSTI
'16841	V											V			V					
' 16843	V		- 5												+					
'16853	V		- 15		*															
'16861			- 3		17							V								
'16863	V		15									V			V					
'16864												V								See III
'16901				7											V					See ITA
'16922	- 01			4																+GTL
'16952	V			V*								V			V				+	Sea Jiir
'18245	V			+																See JTA
'18502				+																See JTA

 [✔] Product available in technology indicated
 ★ Product available as a military device only

DEVICE		BiCMOS				BIPOLAR						CMOS								OTHER
DEVIOL	ABT	ALB	BCT	LVT	ALS	AS	FA	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	HCT	LV	LVC	OTTIL
18504	Strike to be	Up disjoin	uniferation	V	Whed ave	deline in	ed mort	Alice arthur	cuel Clis	JZ \$1,1000	routing)	4 199	product	Manney (1)	lector/o	no leaffeet	N		-	See JTA
18512	-			+													-			See JTA
18514	-			+																See JT/
18516	-			+											- 1				7	See JT
18640	V			+														Amount of the		See JT
18646				+											- "					See JT
18652				+								-2/								See JT
25245	V		V									- 2			- ^					
29821			V		V						-	- 2								
29823	2		V		*															
29827	15		V		V										4					
29828	10				V							- 04								
29833					V															766.
29834			V												91					1.5
29841			V	24	V										16					
29843	1/4		V									-								
29854			V												90					
29863			V		V										*					
32245	V											100			. ^					-
32316	V											10	D/de-		- 1					
32318	V										- 100	1 5%			20					
32501	V														10					
32543	V														-			-		
72211L												V		-	-					See F
72221L	0											V								See F
72231L	100										9	V			7				1 *	See F
72241L												V								See F
161284												100							+	
162240	1			1/							- 7	-			+				100	
162244	V			V							1	13			V				+	✓ LV

DEVICE		BiC	MOS								CMOS									OTHER
DEAICE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	НСТ	LV	LVC	OTHER
'162245	V			V											~				+	∠ LVCR
'162260	V														~					
'162268															~					
'162269															~					✓ ALVCHR
'162280															~					
'162282															+					
'162344															~					
'162373				+																
'162374				+																
'162409															~					
'162460	~																			
'162500	~																			
'162501	~																			194
'162525															~					
'162540															+					4
'162601	1														V					
'162721															~					
'162820															~					
'162821															+					
'162823	~																			
'162825	~																			
'162827	~														V					
'162830															V					
'162831															+					
'162841	140	taxa) n	inen out	. 6	duct plan	ried to a	Ligantà e	07,00				+								
'164245	obla in la	177400	and notice!	0.19	dri ma	lable in n	Character.	Last private	read Calif	S (TARON	arisen!	3. 14.	PENNIN	planted in	V					4000 5 11 60
'182245				+										-						See JTAG
'182502	V			+	-															See JTAG
'182504	V			V				-		-	-			-						See JTAG
'182512				+				-			-									See JTAG

[✔] Product available in technology indicated

Product available in reduced-noise advanced CMOS (11000 series)
 New product planned in technology indicated
 Product planned as a military device

^{*} Product available as a military device only

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DEMOSE.		BiCI	MOS								CMOS								ATUED	
DEVICE	ABT	ALB	BCT	LVT	ALS	AS	F	LS	S	TTL	AC	ACT	AHC	AHCT	ALVC	HC	НСТ	LV	LVC	OTHER
182514	Settle in t		Policy	+	THE REAL PROPERTY.		ognieuw	Gan galan	mand Cha	of Made	District Co.		110000	Montest b	1	an pergent				See JTA
182516				+																See JTA
182640				+																See JTA
182646	V			+						-			-							See JTA
182652	V			+																See JTA
Product avai	ilable in te lable as a	echnology military d	indicated evice only	• Pr	roduct ava	ailable in r	educed-n military d	oise adva levice	nced CM(OS (11000	series)	+ Nev	w product	planned in	technolog	gy indicat	ed			

DEVICE SELECTION GUIDE	1
FUNCTIONAL CROSS-REFERENCE	3
FUNCTIONAL INDEX	2
LOGIC OVERVIEW	1

MERVAEVO DIBO.

PUNCTIONAL INCEX

DEVICE SELECTION CUIDS

SECTION 4 DEVICE SELECTION GUIDE

CONTENTS

ABT - Advanced BiCMOS Technology	4-5
ABTE/ETL - Advanced BiCMOS Technology/Enhanced Transceiver Logic	4–11
AC/ACT - Advanced CMOS Logic	4-13
AHC/AHCT - Advanced High-Speed CMOS Logic	4–19
ALB - Advanced Low-Voltage BiCMOS	4-23
ALS - Advanced Low-Power Schottky Logic	4-25
ALVC - Advanced Low-Voltage CMOS Technology	4-31
AS – Advanced Schottky Logic	4–35
BCT - BiCMOS Bus-Interface Technology	4–39
64BCT – 64-Series BiCMOS Technology	4-43
BTA – Bus-Termination Arrays	4-45
BTL/FB+ - Backplane Transceiver Logic	4-47
CBT - Crossbar Technology	4-49
74F – Fast Logic	4-51
FIFO – First-In, First-Out Memories	4–55
GTL - Gunning-Transceiver-Logic Technology	4-59
HC/HCT - High-Speed CMOS Logic	4-61
IEEE 1149.1 (JTAG) Boundary-Scan Logic Devices	4-67
LS – Low-Power Schottky Logic	4-71
LV – Low-Voltage CMOS Technology	
LVC - Low-Voltage CMOS Technology	4-79
LVT – Low-Voltage BiCMOS Technology	
S – Schottky Logic	
SSTL – Series-Stub Terminated Logic	
TTL – Transistor-Transistor Logic	4–91

Refer to the following for MIL column entries:

military package description and availability

CDIP (ceramic dual-in-line package)	CFP (ceramic flat package)	CQFP (ceramic quad flat package)
J = 14/16/20 pins	WA = 14 pins (small outline)	HV = 68 pins
JT = 24/28 pins	W = 14/16/20 pins	HT = 84 pins
	WD = 48/56 pins	HS = 100 pins
schedule	CPGA (ceramic pin grid array)	HFP = 132 pins
✓ = Now	GB = 68/84/120 pins	LCCC (leadless ceramic chip carrier)
+ = Planned	35 - 55 6 17 125 pino	FK = 20/28 pins

应收据文字报查

Transceiver Logic 4-11	
24-A	
4-55	
Wed in consistence of the constitution of the	
03-A	

Refer to the following for MiL column entries:

ndivary pastage decorpions and evaluation

HY = 88 pins HT = 64 pins HS = 100 pins HSP = 132 pins

 $\xi_i 000$ (seedless continio objectmint) PE $_{\rm c} 1000$ plns

ABT Advanced BiCMOS Technology

The ABT family is TI's second generation family of BiCMOS bus-interface products. It is manufactured using the latest 0.8- μ BiCMOS process and provides high drive up to 64 mA and propagation delays below the 5-ns range, while maintaining very low power consumption. ABT products are well suited for live-insertion applications with an $I_{\mbox{off}}$ specification of 0.1 mA.

To reduce transmission-line effects, the ABT family has series-damping resistor options. Furthermore, there are special ABT parts that provide extremely high-current drive (180 mA) to transmit down to $25-\Omega$ transmission lines. Advanced bus functions, such as universal bus transceivers (UBTTM) emulate a wide variety of bus-interface functions. Multiplexing options for memory interleaving and bus upsizing or downsizing also are provided.

The ABT devices can be purchased in octal, Widebus™, or Widebus+™. The Widebus™ and Widebus+™ packages feature higher performance with reduced noise and flow-through pinout for easier board layout. In addition, the Widebus+™ devices have bus-hold circuitry on the inputs to eliminate the need for external pullup resistors for floating inputs.

For ABT data sheets, see the 1994 Advanced BiCMOS Technology Data Book, literature number SCBD002B.

ABT

idina Nou	NO.	DE SONTEN				AVAILAE	BILITY			LITERATURI
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	TQFP	REFERENCE
SN74ABT125	14	Quad Bus Buffer Gate (OE)	V	~	~	V	V			SCBS182C
SN74ABT126	14	Quad Bus Buffer Gate (OE)		~	~	~	+			SCBS183A
SN74ABT240A	20	Octal Buffer/Driver	~	~	~	~	V			SCBS098G
SN74ABT241A	20	Octal Buffer/Driver	~	V	V	~	V			SCBS184C
SN74ABT244A	20	Octal Buffer/Driver	V	V	V	V	V	+		SCBS099H
SN74ABT245B	20	Octal Bus Transceiver	V	~	V	V	V	+		SCBS081F
SN74ABTH245	20	Octal Bus Transceiver		~	V	~	V	+		SCBS663
SN74ABT273	20	Octal D-Type Flip-Flop With Clear	V	V	V	V	V			SCBS185A
SN74ABT373	20	Octal D-Type Transparent Latch	V	1	V	91	+			SCBS155B
SN74ABT374A	20	Octal D-Type Flip-Flop	V	V	V	· /	V			SCBS111F
SN74ABT377A	20	Octal D-Type Flip-Flop With Clock Enable	V	V	V	W V	V			SCBS156D
SN74ABT533A	20	Octal D-Type Transparent Latch	V	V	V	V	V			SCBS186C
SN74ABT534A	20	Octal D-Type Flip-Flop	V	V	V	V	V			SCBS187E
SN74ABT540	20	Octal Buffer/Driver	CAGAILE IN	V	V	V				SCBS188B
SN74ABT541B	20	Octal Buffer/Driver	V	V	V	V	V			SCBS093G
SN74ABT543A	24	Octal Registered Bus Transceiver	V	V	V	V	V			SCBS157D
SN74ABT573A	20	Octal D-Type Transparent Latch	V	V	V	V	V			SCBS190B
SN74ABT574A	20	Octal D-Type Flip-Flop	V	V	V	V	V			SCBS191B
SN74ABT620	20	Octal Bus Transceiver		V	V	V	+			SCBS113B
SN74ABT623	20	Octal Bus Transceiver	vo	V	V	V	V			SCBS114B
SN74ABT640	20	Octal Bus Transceiver	W br	SV 8	V	V	V			SCBS104B
SN74ABT646	24	Octal Registered Bus Transceiver	and	V	V	V	V	+		SCBS068E
SN74ABT646A	24	Octal Registered Bus Transceiver	V	V	V	VV	+			SCBS069E
SN74ABT651	24	Octal Registered Bus Transceiver	q lan	V	V	0.0	+			SCBS083C
SN74ABT652	24	Octal Registered Bus Transceiver		V	V	~	+			SCBS070D
SN74ABT652A	24	Octal Registered Bus Transceiver	V	V	V	V	+			SCBS072D
SN74ABT657A	24	Octal Parity Bus Transceiver	lun s	V	V	+				SCBS192B
SN74ABT821A	24	10-Bit Bus-Interface Flip-Flop	V	V	V	V	+			SCBS193C
SN74ABT823	24	9-Bit Bus-Interface Flip-Flop	V	V	V	V	+			SCBS158C
SN74ABT827	24	10-Bit Buffer/Driver	V	V	V	V	V			SCBS159B
SN74ABT833	24	8-Bit to 9-Bit Parity Bus Transceiver		V	V					SCBS195B

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package) PAH

= 52 pins = 64 pins PAG PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ABT

DEVICE	NO.	FUNCTION					AVAILAE	BILITY			LITERATURI
DEVICE	PINS	7 90887 908 308 909	304	MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	TQFP	REFERENCE
SN74ABT841	24	10-Bit Bus-Interface D-Type Latch		~	V	V	~	+	66 16	10	SCBS196B
SN74ABT841	24	10-Bit Bus-Interface D-Type Latch		~	V	V	~	+	86 18	108	SCBS196B
SN74ABT843	24	9-Bit Bus-Interface D-Type Latch		V	~	~	V.	effuel III	48 16	(8)	SCBS197B
SN74ABT853	24	8-Bit to-9 Bit Parity Bus Transceiver		V	~	~	· V	+	81 84	19	SCBS198C
SN74ABT861	24	10-Bit Bus Transceiver	No		V	V	a b+or	igeR NG	87 88	83	SCBS199A
SN74ABT863	24	9-Bit Bus Transceiver			~	V	~	wirt) jis	81 88	(0)	SCBS201A
SN74ABT2240	20	Octal Buffer and Line/MOS Driver	N	~	~	V	V	wint+3	56 19	ro	SCBS232B
SN74ABT2241	20	Octal Buffer and Line/MOS Driver			~	V	· V	+	48 16	ES	SCBS233A
SN74ABT2244A	20	Octal Buffer and Line/MOS Driver	14	~	~	V	V	V	-91 - 634	6)	SCBS106C
SN74ABT2245	20	Octal Transceiver and Line/MOS Dri	ver	~	V	V	1 V	dgefi #8	56 16-	89	SCBS234B
SN74ABT2373	20	Octal D-Type Transparent Latch	10		V	V	8 V 9	V	-81 BB	52	Call
SN74ABT2827	24	10-Bit Buffer/Driver With Series Resi	stors		V	V	Bus Tre	me9 #8	er ea	57	SCBS648
SN74ABT2952A	24	Octal Registered Bus Transceiver			V :	~	V	+	-05 88 -	13	SCBS203A
SN74ABT5400A	28	11-Bit Line/Memory Driver	N		0	V	nordace	Bit Bus-	-81 88	83	SCBS661
SN74ABT5401	28	11-Bit Line/Memory Driver			0	V	eastrein	-ewill file	31 86	838	SCBS235A
SN74ABT5402A	28	12-Bit Line/Memory Driver				V	revhCh	eltue HB	S6 18-	85	SCBS660
SN74ABT5403	28	12-Bit Line/Memory Driver				V	newhility	etne le	55 18-	825	SCBS236A
SN74ABT16240	48	16-Bit Buffer/Driver		V			V	V	os aa	AB	SCBS095E
SN74ABT16241	48	16-Bit Buffer/Driver		V	Trensor	auti yiha		V	St Du	33	SCBS096E
SN74ABT16244A	48	16-Bit Buffer/Driver	W	V	riotaJ	eq/T-C	V	V	S V	12	SCBS073E
SN74ABTH16244	48	16-Bit Buffer/Driver			rioteJ	eq/T-0	V	V	81 +08	E8	SCBS677A
SN74ABT16245A	48	16-Bit Bus Transceiver		V	Transce	urly Bus	V	V	UC VIII	83	SCBS300A
SN74ABTH16245D	48	16-Bit Bus Transceiver				191	V	V	· V	63	SCBS662D
SN74ABT16260	56	12-to-24 Multiplexed D-Type Latch	+	V	roviso	STEERS	V	Blt. Regis	-86 16-	Sã	SCBS204A
SN74ABT16373A	48	16-Bit D-Type Transparent Latch		V		1808iver	V	V	24 25	34	SCBS160A
SN74ABT16374A	48	16-Bit D-Type Flip-Flop	19	V		181	V	V	100 36-	8.0	SCBS205A
SN74ABTH16374	48	16-Bit D-Type Flip-Flop	N	190	Exchae	eu8 leav	evi+tro	4+6	-Bt 08	81	Call
SN74ABT16460	56	4-to-1 Multiplexed/Demultiplexed Transceiver	1	160	nerlock	nual Ison	~	4	61 08 no one	81	SCBS207B
SN74ABT16470	56	16-Bit Registered Bus Transceiver			woulan	on Torre	V	Julia eti	se nor	28	SCBS085C
SN74ABT16500B	56	18-Bit Universal Bus Transceiver		minds	back and	uch car	V	V	21 04	1.00	SCBS057E
SN74ABT16501	56	18-Bit Universal Bus Transceiver					V	V			SCBS086B
ommercial packa	age de	escription and availability			1/28	lidalla	rs lose	and Dept	orob er	soloac	Satorozumi
DIP (plastic dual-in-line pac = 14/16/20 pins		QFP (plastic quad flat package) RC = 52 pins	SOT (a	DBV =	plastic thin	quad flat	80/2	6979 (a) 18 - 38 19 - 30 19 - 30	PW = 8/14/ DGG = 48/56	16/20/24/28 3/64 pins	1 = 2428 pm
LCC (plastic leaded chip ca N = 20/28/44/52/68/84 pins		SOIC (small-outline integrated circuit)		PAH PAG PM PN	= 52 pin = 64 pin = 64 pin = 80 pin	18 18 18	entro-Ken entro-Ken entro Bryst etchstesk		TVSOP (thin DGV = 14/16 DBB = 80/10	3/20/24/48/	outline package) 56 pins
<pre>chedule / = Now - = Planned</pre>		SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins		PCA, PZ PCB	Z = 100 pi = 120 pi				MIL – refer to package desc		



ABT

MUTANTIL	NO.	YTUBARAVA					AVAILAB	ILITY			LITERATURE
DEVICE	PINS	FUNCTION		MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	TQFP	REFERENCE
SN74ABT16501	56	18-Bit Universal Bus Transceiver	W		riofs.i	D-Type	V	V	24 16		SCBS086B
SN74ABTH16501	56	18-Bit Universal Bus Transceiver	10		Lalon	D-Type	eos + sini	eu(+18-0	24 1		Call
SN74ABT16540	48	16-Bit Buffer/Driver	100		dola.	l eqr/T-(V	V	24 9		SCBS208A
SN74ABT16541	48	16-Bit Buffer/Driver	No.		10vleder	ranī sut	V	· /	24 8		SCBS118B
SN74ABT16543	56	16-Bit Registered Bus Transceiver		~		191	V	V	24 1		SCBS087B
SN74ABT16600	56	18-Bit Universal Bus Transceiver				70	~	V	84 9		SCBS209A
SN74ABT16601	56	18-Bit Universal Bus Transceiver	10	V	revirO	80Me	V	V	20 0	0	SCBS210B
SN74ABT16623	48	16-Bit Bus Transceiver			Driver-	SOME	V	etal Bulle	0 08	. 1	SCBS211A
SN74ABT16640	48	16-Bit Bus Transceiver	30	V	JevhC	SOME	V	citue lato	20 0	All	SCBS107B
SN74ABT16646	56	16-Bit Registered Bus Transceiver	10	V	HO SON	Neat Lines	V	etal Truns	20 0	8	SCBS212A
SN74ABT16652	56	16-Bit Registered Bus Transceiver		V	riote	1 Ineres	V	ctal D-Typ	20 0	3	SCBS215A
SN74ABT16657	56	16-Bit Parity Bus Transceiver		store	des Rost	Yith Ser	V	V	24 12	7	SCBS103A
SN74ABT16821	56	20-Bit Bus-Interface Flip-Flop			101/03	e Transc	e V	V	0 15	AS	SCBS216A
SN74ABT16823	56	18-Bit Bus-Interface Flip-Flop		V		teviro	v V oV	V	28 17	A0	SCBS217B
SN74ABTH16823	56	18-Bit Bus-Interface Flip-Flop				revirO	V	V -	284 1		SCBS664
SN74ABT16825	56	18-Bit Buffer/Driver				Orlyan	V	V	28 10	AS	SCBS218A
SN74ABTH16825	56	18-Bit Buffer/Driver				revirio	yoteM	leni t ile-	+33	8	Call
SN74ABT16827A	56	20-Bit Buffer/Driver	10				ne+Gh	tu#18-	48 16	(1)	Call
SN74ABT16833	56	Dual 8-Bit to 9-Bit Parity Bus Transceiv	er				~	eltu 8 ville	48 18	ta	SCBS097C
SN74ABT16841	56	20-Bit Bus-Interface D-Type Latch	16	V			V	eltuS #8-t	48 11	Al-4	SCBS222A
SN74ABT16843	56	18-Bit Bus-Interface D-Type Latch					~	V	48 18	844	SCBS223B
SN74ABT16853	56	Dual 8-Bit to 9-Bit Parity Bus Transceiv	er			10	V	181 Bus	1 84	ABI	SCBS153A
SN74ABT16863	48	18-Bit Bus Transceiver				10	/ V	su8 (184	N. SA	2460	SCBS225A
SN74ABT16952	56	16-Bit Registered Bus Transceiver	No	+	Holsi	D-Tyge	V	V	60 13	08	SCBS082B
SN74ABT25245	24	25-Ω Octal Bus Transceiver	No		1	V	зе Тена	yT-0 184	48 10	AET	SCBS251B
SN74ABT32245	100	36-Bit Bus Transceiver	10	V		qo	H-giFl ed	yT-0 MH	48 16	V	SCBS228C
SN74ABT32316	80	16-Bit Tri-Port Universal Bus Exchange	er	V		qo	HqH sq	y7-0 18-	1 85	V-18	SCBS179A
SN74ABT32318	80	18-Bit Tri-Port Universal Bus Exchange	er		beau	lgālums	Olbexelo	üluM t-ol	h	V	SCBS180A
SN74ABT32501	100	36-Bit Universal Bus Transceiver	. Les	V				YS VIRQUENTS		V	SCBS229B
SN74ABT32543	100	36-Bit Registered Bus Transceiver		V	10460	ansil a	el benste	NORTH THE	86 14	V	SCBS230B
SN74ABT162244	48	16-Bit Buffer/Driver With Series Resisto	ors	V	19718	nenant	V	V	11 86	FICE	SCBS238B

commercial package description and availability

PDIP (plastic dual-in-line package)

 $N = 14/16/20 \, \text{pins}$

NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now

+ = Planned

QFP (plastic quad flat package)

RC = 52 pins

PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)

D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins PAH

PAG

PM = 64 pins

PN = 80 pins

PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package)

PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ABT

	NO.	TIMOTON				AVAILAE	BILITY			LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	TQFP	REFERENCE
SN74ABT162245	48	16-Bit Bus Transceiver With Series Resistors	~			~	V			SCBS239C
SN74ABT162260	56	12-Bit to 24-Bit Multiplexed D-Type Latch With Series Resistors		1		~				SCBS240A
SN74ABT162460	56	4-to-1 Multiplexed/Demultiplexed Registered Transceiver With Series Resistors				~				SCBS241A
SN74ABT162500	56	18-Bit Universal Bus Transceiver With Series Resistors				~	+			SCBS242B
SN74ABT162501	56	18-Bit Universal Bus Transceiver With Series Resistors				~	V			SCBS243B
SN74ABT162601	56	18-Bit Universal Bus Transceiver With Series Resistors				~	V			SCBS247C
SN74ABT162823	56	18-Bit Bus-Interface Flip-Flop With Series Resistors				~				SCBS473A
SN74ABT162825	56	18-Bit Buffer/Driver With Series Resistors				~	+			SCBS474A
SN74ABT162827	56	20-Bit Buffer/Driver With Series Resistors				~	V			SCBS248C
SN74ABT162841	56	20-Bit Bus-Interface D-Type Latch With Series Resistors			10	V	~			SCBS665

commercial package description and availability

QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins SOT (small-outline transistor) DBV = 5 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins NP = 28 pins TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins = 64 pins = 80 pins PM PN schedule PCA, PZ = 100 pins PCB = 120 pins SSOP (shrink small-outline package) ✓ = Now MIL - refer to page 4-1 for military DB = 14/16/20/24/28/30/38 pins + = Planned DL = 28/48/56 pins package description and availability



TWA

		12-Bit to 24-Bit Multiplexed O-Type Latch. With Series Resistors	
		20-Bit Buller/Driver With Series Residers	

validallava has collaborah epistona lolarenmen

PDP (please dout-in-time participal)

If = hairbord pins

INT = 24228 pins

INT = 26 pins

PLDC (please bedded only carried)

INT = 200004102108084 pins

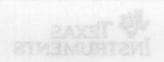
politicalization

GPP disable qualified providing RD = 12 pino PH = 10 pino PO = 100/132 pino SOIIC (amal-ophia attagrator chall II = 8/14/18 pino BI = 8/14/18 pino

(fluorio kotar)

TOT (amint outline harelete)
enty is 70%
enty is 70%
enty is 70%
enty is 80%
enty is 80%
enty is 80%
enty is 90%
e

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ABTE/ETL Advanced BiCMOS Technology/ Enhanced Transceiver Logic

ABTE has wider noise margins and is backward compatible with existing TTL logic. ABTE devices support the VME64-ETL specification with tight tolerances on skew and transition times. ABTE is manufactured using the latest 0.8- μ BiCMOS process by providing high drive up to 90 mA. Other features include a bias pin and internal pullup resistors on control pins for maximum live-insertion protection. Bus-hold circuitry eliminates external pullup resistors on the inputs and series-damping resistors on the outputs to damp reflections.

For ABTE/ETL data sheets, see the 1997 *GTL, BTL, and ETL Logic Data Book*, literature number SCED004.

ABTE/ETL

DEVICE STATES	NO.	FINATION		VAILABIL	TY	LITERATURE
DEVICE	PINS	FUNCTION	MIL	SSOP	TSSOP	REFERENCE
SN74ABTE16245	48	16-Bit Incident-Wave Switching ETL Bus Transceiver	V	~	V	SCBS226F
SN74ABTE16246	48	11-Bit Incident-Wave Switching ETL Bus-Control Transceiver With 3-State and Open-Collector Outputs		~	~	SCBS227D

gic. ABTE devices support the VME64-ETL specification with tight lerances on skew and transition times. ABTE is manufactured using the test 0.8-µ BiCMOS process by providing high drive up to 90 mA. Other attures include a bias pin and internal pullup resistors on control pins for eximum live-insertion protection. Bus-hold circuitry eliminates external altup resistors on the inputs and serice-damping resistors on the outputs to amp reflections.

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins	QFP (plastic quad flat package) RC = 52 pins PH = 80 pins	SOT (small-outline transistor) DBV = 5 pins	TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins
NP = 28 pins	PQ = 100/132 pins	TQFP (plastic thin quad flat package)	TVSOR (this year amall suttling analyses)
PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins	SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins	PAH = 52 pins PAG = 64 pins PM = 64 pins PN = 80 pins	TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins
✓ = Now+ = Planned	SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins	PCA, PZ = 100 pins PCB = 120 pins	MIL – refer to page 4–1 for military package description and availability



AC/ACT Advanced CMOS Logic

The ACL family of devices is manufactured in 1- μ CMOS and has more than 70 functions, including gates, flip-flops, drivers, counters, and transceivers. The ACL family is a reliable, low-power logic family with 24-mA output drive.

Included in the family are standard end-pin products and center-pin V_{CC} and ground-configuration products with output-edge control (OEC™) circuitry. The OEC™ circuitry, available only with the center-pin products, helps reduce simultaneous switching noise associated with high-speed logic. Included in the center-pin products are 16-, 18-, and 20-bit bus-interface functions packaged in 48- and 56-pin shrink small-outline packages (SSOP) and thin shrink small-outline packages (TSSOP). These packages allow the designer to double functionality in the same circuit-board area or reduce the circuit-board area by half.

AC devices offer CMOS-compatible inputs and ACT devices offer TTL-compatible inputs.

For AC/ACT data sheets, see the 1997 AC/ACT CMOS Logic Data Book, literature number SCAD001D.

AC

Canada be	NO.	DEALOR SELL			AVAILABI	LITY		LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	TSSOP	REFERENCE
SN74AC00	14	Quad 2-Input NAND Gate	~	~	~	V	V	SCAS524C
SN74AC04	14	Hex Inverter	V	V	V	~	V	SCAS519C
SN74AC08	14	Quad 2-Input AND Gate	V	~	V	V	V	SCAS536B
SN74AC10	14	Triple 3-Input NAND Gate	V	~	V	V	V	SCAS529B
SN74AC11	14	Triple 3-Input AND Gate	V	V	~	V	V	SCAS532B
SN74AC14	14	Hex Inverter With Schmitt Trigger	V	V	V	V	V	SCAS522C
SN74AC32	14	Quad 2-Input OR Gate	V	V	V	V	V	SCAS528B
SN74AC74	14	Dual D-Type Flip-Flop	O/Van	TV	~	V	V	SCAS521C
SN74AC86	14	Quad 2-Input Exclusive-OR Gate	ONV C	V	V	V	V	SCAS533A
SN74AC240	20	Octal Buffer/Driver	OVE	V	V	V	V	SCAS512C
SN74AC241	20	Octal Buffer/Driver		V	V	V	V	SCAS513C
SN74AC244	20	Octal Buffer/Driver	V	V	~	V	V	SCAS514C
SN74AC245	20	Octal Bus Transceiver	V	V	V	V	V	SCAS461D
SN74AC373	20	Octal D-Type Transparent Latch	V	V	V	V	V	SCAS540B
SN74AC374	20	Octal D-Type Flip-Flop	V	V	V	V	V	SCAS543B
SN74AC533	20	Octal D-Type Transparent Latch		V	V	V	V	SCAS555A
SN74AC534	20	Octal D-Type Flip-Flop		V	V.	V	V	SCAS554A
SN74AC563	20	Octal D-Type Transparent Latch	unda .	V	V	V	V	SCAS552A
SN74AC564	20	Octal D-Type Flip-Flop	Litization	V	V	V	V	SCAS551A
SN74AC573	20	Octal D-Type Transparent Latch		V	~	V	V	SCAS542B
SN74AC574	20	Octal D-Type Flip-Flop	V	AV	V	V	V	SCAS541B
74AC11000	16	Quad 2-Input Positive-NAND Gate	TL-co	TV	V			SCLS054A
74AC11004	20	Hex Inverter		V	V	~		SCAS033B
74AC11008	16	Quad 2-Input Positive-AND Gate	OA 10	V	V		V	SCAS014C
74AC11032	14, 16	Quad 2-Input Positive-OR Gate	nutava	~	~	~		SCAS007C
74AC11074	14	Dual D-Type Flip-Flop		V	V		~	SCAS499A
74AC11086	16	Quad 2-Input Exclusive-OR Gate		V	V			SCAS081A
74AC11138	16	3-to-8 Decoder/Demultiplexer		V	V		~	SCAS042B
74AC11139	16	Dual 2-to-4 Decoder/Demultiplexer		V	V		~	SCAS070B
74AC11240	24	Octal Buffer/Driver		V	V	~		SCAS448A
74AC11244	24	Octal Buffer/Driver		V	V	V	V	SCAS171A

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

= Now + = Planned QFP (plastic quad flat package)
RC = 52 pins
PH = 80 pins
PQ = 100/132 pins

SOIC (small-outline integrated circuit)

D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins PAH = 52 pins
PAG = 64 pins
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins
PCB = 120 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/18/20/24/48/56 pins DBB = 80/100 pins



DEVICE	NO. PINS	FUNCTION	MIL PDIP	SOIC	SSOP	TSSOP	LITERATURE REFERENCE
74AC11245	24	Octal Bus Transceiver	ds0 0 V M	V	OV A	V	SCAS010B
74AC11257	20	Quad 2-to-1 Data Selector/Multiplexer		alnovní z	V	V	SCAS049B
74AC11373	24	Octal D-Type Transparent Latch	eta D V A	V	OV		SCAS213A
74AC11374	24	Octal D-Type Flip-Flop	elad OVAL	V	~	1	SCAS214A
74AC11520	20	8-Bit Identity Comparator	elsi) VA	ugni č eto	at the		SCAS025C
74AC11652	28	Octal Registered Bus Transceiver	repphT alm/to2 🗸 N/	V	a Ha		SCAS088A
74AC16240	48	16-Bit Buffer/LineDriver	stic9 RO1	ed 2-Inpu	V	1	SCAS234B
74AC16244	48	16-Bit Buffer/Driver	qoR-qiP	al D-Type	OV S	· V	SCAS120A
74AC16245	48	16-Bit Bus Transceiver	ansi) RO-svlaubx3)	ed 2-Input	OV :	V	SCAS235A
74AC16373	48	16-Bit D-Type Transparent Latch	tevhO	Avoituel to	0V 0	2	SCAS121B
74AC16374	48	16-Bit D-Type Flip-Flop	Driver	tellus la	0V 0		SCAS123B
74AC16472	56	16-Bit Latched Bus Transceiver	Driver	teettuä le	0 VO	2	SCAS165A
74AC16543	56	16-Bit Registered Bus Transceiver	naviacens	niT eud tel	0V 0	2	SCAS125B
74AC16620	48	16-Bit Bus Transceiver	rists,) invingenes?	sqyT-Q les	00V 0	2	SCAS239A
74AC16640	48	16-Bit Bus Transceiver	qcR-qiR :	eqy(T-Q ts	OV 0	2	SCAS240A
74AC16646	56	16-Bit Registered Bus Transceiver	Transparent Laten	agyîf-G lai	V	9	SCAS241A
74AC16652	56	16-Bit Registered Bus Transceiver	Flip-Flip	sq/f-G la	ov o	2	SCAS242A
74AC16823	56	18-Bit Bus-Interface Flip-Flop	riots. I the sugarent T	at D-Type	000	8	SCAS243A
SCASSAGA	70	4 4 4	Fig-Figs	eq/T-G lei	bO 0	2	SHYAACTS64

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package) RC = 52 pins

PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins PAH PAG PM = 64 pins PN = 80 pins

PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)

PW = 8/14/16/20/24/28 pins

DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ACT

DEVICE	NO.	FUNCTION		,	AVAILABILITY			LITERATURE
DEVIOL	PINS	ices olds 4les Janetton	MIL	PDIP	SOIC	SSOP	TSSOP	REFERENCE
SN74ACT00	14	Quad 2-Input NAND Gate	+	V	V	V	V	SCAS523A
SN74ACT04	14	Hex Inverter	revelop V no	V	OV	V	09/	SCAS518A
SN74ACT08	14	Quad 2-Input AND Gate	no 🗸 h	~	TW	V	V	SCAS535A
SN74ACT10	14	Triple 3-Input NAND Gate	~	V-	V	V	W	SCAS526A
SN74ACT11	14	Triple 3-Input AND Gate	~	~	0	V	00	SCAS531A
SN74ACT14	14	Hex Inverter With Schmitt Trigger	savie+ne	1	V	V	800	SCAS557B
SN74ACT32	14	Quad 2-Input OR Gate	+	· /	~	100	111	SCAS530A
SN74ACT74	14	Dual D-Type Flip-Flop	V	~	V	NV	814	SCAS520C
SN74ACT86	№ 14	Quad 2-Input Exclusive-OR Gate	~	~	V	V	814	SCAS534A
SN74ACT240	20	Octal Buffer/Driver	rice 🗸 and	~	W-0		814	SCAS515B
SN74ACT241	20	Octal Buffer/Driver	V	QV-qI	V	V	814	SCAS516B
SN74ACT244	20	Octal Buffer/Driver	V	V	V	V	8 V	SCAS517B
SN74ACT245	20	Octal Bus Transceiver	novie v no	V	V	11 V	V	SCAS452C
SN74ACT373	20	Octal D-Type Transparent Latch	V	V	V	· ·	814	SCAS544B
SN74ACT374	20	Octal D-Type Flip-Flop	V	100	V	V	814	SCAS539C
SN74ACT533	20	Octal D-Type Transparent Latch	havisoens	V	V	V	V	SCAS553A
SN74ACT534	20	Octal D-Type Flip-Flop	теујеоеле	V	V	100	1 V	SCAS556A
SN74ACT563	20	Octal D-Type Transparent Latch	qoff-	V	e V B	V	V	SCAS550A
SN74ACT564	20	Octal D-Type Flip-Flop		V	V	V	V	SCAS549A
SN74ACT573	20	Octal D-Type Transparent Latch	V	V	~	V	V	SCAS538B
SN74ACT574	20	Octal D-Type Flip-Flop		V	~	V	V	SCAS537A
SN74ACT1284	20	7-Bit IEEE P1284 Driver/Receiver			~	V		SCAS459B
74ACT11004	20	Hex Inverter		V	~	V	+	SCAS215A
74ACT11008	16	Quad 2-Input Positive-AND Gate		V	~		V	SCAS013C
74ACT11032	14, 16	Quad 2-Input Positive-OR Gate		V	~	V	V	SCAS008C
74ACT11074	14	Dual D-Type Flip-Flop		V	V	V		SCAS046A
74ACT11139	16	Dual 2-to-4 Decoder/Demultiplexer		V	~		V	SCAS175A
74ACT11240	24	Octal Buffer/Driver		V	~	V		SCAS210A
74ACT11244	24	Octal Buffer/Driver		V	~	V	V	SCAS006C
74ACT11245	24	Octal Bus Transceiver		V	V	V	V	SCAS031C
74ACT11257	20	Quad 2-to-1 Data Selector/Multiplexer		V	V	V		SCAS053B

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule ✓ = Now + = Planned

QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package) = 52 pins = 64 pins PAH PAG

PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins



ACT

DEVICE	NO. PINS	FUNCTION	HOTOM	PDIP	AVAILABI	LITY	TSSOP	LITERATURE REFERENCE
74ACT11286	14	9-Bit Parity Generator/Checker	Bus Transceiver	V	1948	Bug Bug	5	SCAS069B
74ACT11373	24	Octal D-Type Transparent Latch	Hotel Latch	V	V	-03V	13	SCAS015B
74ACT11374	24	Octal D-Type Flip-Flop		~	V	100V	8	SCAS217A
74ACT11652	28	Octal Registered Bus Transceiver	1	wiscens	Tev	1-81 8	13	SCAS087A
74ACT11656	28	Octal Parity Bus Transceiver	1	evistens	V	1-81 8	8	SCAS460A
74ACT16240	48	16-Bit Buffer/Driver	neviere V	ered Bus	isigo/i N	-81V 8	8	SCAS137C
74ACT16241	48	16-Bit Buffer/Driver	Flyge Latch With Se	l soshdi	nl-cu/B fit	1-05V 8	5	SCAS189A
74ACT16244	48	16-Bit Buffer/Driver	V			V	V	SCAS116B
74ACT16245	48	16-Bit Bus Transceiver	V			V	V	SCAS097B
74ACT16254	64	32-to-16 VL Bus Multiplexer/Demultiplexer					V	SCAS527A
74ACT16373	48	16-Bit D-Type Transparent Latch	V		MUH	V		SCAS122C
74ACT16374	48	16-Bit D-Type Flip-Flop	V			V		SCAS124B
74ACT16470	56	16-Bit Registered Bus Transceiver				V		SCAS237A
74ACT16474	56	18-Bit Registered Bus Transceiver				V		SCAS238A
74ACT16475	56	16-Bit Registered Transceiver				V		SCAS198A
74ACT16540	48	16-Bit Buffer/Driver				V		SCAS186A
74ACT16541	48	16-Bit Buffer/Driver				V		SCAS208A
74ACT16543	56	16-Bit Registered Bus Transceiver	~			V	V	SCAS126B
74ACT16544	56	16-Bit Registered Bus Transceiver				V		SCAS161A
74ACT16620	48	16-Bit Bus Transceiver				V		SCAS184A
74ACT16623	48	16-Bit Bus Transceiver				V		SCAS152A
74ACT16640	48	16-Bit Bus Transceiver				V		SCAS173A
74ACT16646	56	16-Bit Registered Bus Transceiver				~		SCAS127B
74ACT16648	56	16-Bit Registered Bus Transceiver				V		SCAS188A
74ACT16651	56	16-Bit Registered Bus Transceiver				V		SCAS449A
74ACT16652	56	16-Bit Registered Bus Transceiver	V			V		SCAS128C
74ACT16657	56	Dual 8-to-9 Bit Parity Bus Transceiver				~		SCAS164A
74ACT16821	56	20-Bit Bus-Interface Flip-Flop				V		SCAS176A
74ACT16823	56	18-Bit Bus-Interface Flip-Flop				V		SCAS160A
74ACT16825	56	18-Bit Buffer/Driver				V		SCAS155B
74ACT16827	56	20-Bit Buffer/Driver				V	4 3 1 7	SCAS163A

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

+ = Planned

✓ = Now

QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH PAG = 52 pins = 64 pins PM PN = 64 pins

PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins

DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ACT

DEVICE		NO. PINS		FUNCTION		MIL	PDIP	AVAILABII	LITY	TSSOP	LITERATURE
74ACT16833	*LAGIC	56	Dual 8-to-9 Bit Parity	/ Bus Transceiver		MIL	PUIP	SOIC	55UF	13509	SCAS166A
74ACT16841		56	20-Bit Bus-Interface		da	e J finens	nanerT	sovT-fi is	V	18 V	SCAS174A
74ACT16861		56	20-Bit Bus Transceiv				oR-glR	orn/T-/T lo	V	he.	SCAS197B
74ACT16863		56	18-Bit Bus Transceiv		Next	Fennse	n B box	of Develope	V	98	SCAS162B
74ACT16864		56	18-Bit Bus Transceiv		1996	no done	trus Trus	notyport in Luksell to	V	66	SCAS244A
74ACT16952		56	16-Bit Registered Bu			19 /1908	40011 CSA	a yaras ir sa	V	Dis.	SCAS159C
74ACT16952 74ACT162841		56			oriae Basistara		TOWNS.	nation to	31+	85	Call
	V		-	D-Type Latch With Se	eries nesisiors		BALLIO	HOTIVE IN		08	

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins	QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins	SOT (small-outline transistor) DBV = 5 pins TQFP (plastic thin quad flat package)	TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins
PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins	SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins	PAH = 52 pins PAG = 64 pins PM = 64 pins PN = 80 pins	TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins
✓ = Now + = Planned	SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins	PCA, PZ = 100 pins PCB = 120 pins	MIL – refer to page 4–1 for military package description and availability



AHC/AHCT Advanced High-Speed CMOS Logic

The AHC/AHCT logic family provides a natural migration for HCMOS users who need more speed for low-power, low-noise, and low-drive applications. The AHC logic family consists of basic gates, medium-scale integrated circuits, and octal functions fabricated using the EPIC1-S process that produces high performance at low cost. In addition, TI offers a new single-gate solution in its MicroGate family, designated with 1G in the device name.

Performance characteristics of the AHC family are:

- Speed With typical propagation delays of 5.2 ns (octals), which is about three times faster than HC devices, AHC devices are the quick and quiet solution for higher-speed operation.
- Low noise The AHC family allows designers to combine the low-noise characteristics of HCMOS devices with today's performance levels without the overshoot/undershoot problems typical of higher-drive devices usually required to get AHC speeds.
- Low power The AHC family, by using CMOS technology, exhibits low power consumption (40-μA maximum static current, half that of HCMOS).
- Drive Output-drive current is ±8 mA at 5-V V_{CC} and ±4 mA at 3.3-V V_{CC}.
- Packaging AHC devices are available in D and DW (SOIC), DB (SSOP), N (PDIP), and PW (TSSOP) packages, and planned in the DGV (TVSOP).
 Selected AHC devices are available in military versions (SN54AHCXX).

Using TI products offers several business advantages:

- Competitive advantage AHC and VHC devices have equivalent specifications; therefore, AHC devices are "drop in" replaceable. With TI's production capacity, delivery performance, and competitive prices, AHC devices are among the most economical, easy-to-use, and easy-to-get logic products.
- Alternate source TI has arrangements for one or more alternate sources for AHC devices.

For AHC/AHCT data sheets, see the 1996 AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book, literature number SCLD004.

AHC

DEVICE	NO.	FUNCTION			AVAII	LABILITY				LITERATURE
DEVICE	PINS	PONCTION	MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	SOT	REFERENC
SN74AHC1G00	5	Single 2-Input Positive-NAND Gate							~	SCLS313A
SN74AHC1G04	5	Single Inverter Gate							V	SCLS318B
SN74AHC1GU04	5	Unbuffered Single Inverter Gate							V	SCLS343D
SN74AHC1G08	5	Single 2-Input Positive-AND Gate	bale A	110	EFA				~	SCLS314A
SN74AHC1G14	5	Single Schmitt-Trigger Inverter Gate		an I see.	59 12 07 19				+	SCLS321B
SN74AHC1G32	5	Single 2-Input Positive-OR Gate	190	們信	FOA				~	SCLS317A
SN74AHC1G86	5	Single 2-Input Exclusive-OR Gate	da E	20	S.O.M				+	SCLS323B
SN74AHC00	. 14	Quad 2-Input NAND Gate	+	V	V	V	~	V		SCLS227A
SN74AHC02	14	Quad 2-Input NOR Gate	deat 75				~	V		SCLS254C
SN74AHC04	14	Hex Inverter	V	V	V	V	~	V		SCLS231C
SN74AHCU04	14	Unbuffered Hex Inverter	V	V	~	V	~	V		SCLS234A
SN74AHC08	14	Quad 2-Input AND Gate	+	V	V	V	~			SCLS236A
SN74AHC14	14	Hex Inverter With Schmitt Trigger	V	V	V	V	V			SCLS238B
SN74AHC32	14	Quad 2-Input OR Gate	V	V	~	V	V	V		SCLS247A
SN74AHC74	14	Dual D-Type Flip-Flop With Preset and Clear	~	~	~	~	V			SCLS255B
SN74AHC86	2114	Quad Exclusive-OR Gate	V	1	0 V 8	V	V			SCLS249A
SN74AHC125	14	Quad Bus Buffer Gate (OE)	eia# a	V	V	V	V			SCLS256B
SN74AHC126	14	Quad Bus Buffer Gate (OE)	V	V	OV	V	V			SCLS257B
SN74AHC138	16	3-to-8 Decoder/Demultiplexer	edT-l	V	10 V 8	V	V	V		SCLS258C
SN74AHC139	16	Dual 2-to-4 Line Decoder/Demultiplexer	stics o	V	N.V	V	V	V		SCLS259C
SN74AHC157	16	Quad 2-to-1 Data Selector/Multiplexer	avo en	1 Hor	HW+	+	+			SCLS345
SN74AHC158	16	Quad 2-to-1 Data Selector/Multiplexer	SUBILY F	+	+	+	+			SCLS346
SN74AHC240	20	Octal Bus Buffer/Driver	V	V	V	V	V	THE T		SCLS251A
SN74AHC244	20	Octal Buffer/Driver	V	V	V	V	V	V		SCLS226C
SN74AHC245	20	Octal Bus Transceiver	V	V	V	V	V	V		SCLS230B
SN74AHC257	16	Quad 2-to-1 Data Selector/Multiplexer		+	+	+	+		T	SCLS349
SN74AHC258	16	Quad 2-to-1 Data Selector/Multiplexer	A PRESE	+	+	+	+			SCLS350
SN74AHC373	20	Octal D-Type Transparent Latch	V	V	V	V	V			SCLS235B
SN74AHC374	20	Octal D-Type Flip-Flop	lo V	bov 1	V	V	V			SCLS240B
SN74AHC540	20	Inverting Octal Bus Buffer	OSV.	V	V	V	V			SCLS260C
SN74AHC541	20	Octal Buffer/Driver	Vo	V	OV	V	V			SCLS261F
ATA manho acti	III and the second	escription and availability	n capac	oltoub	ong					COLOLOII
DIP (plastic dual-in-line p = 14/16/20 pins T = 24/28 pins P = 28 pins	29.29.1.2	QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins	DBV =	DUTTE ME	transistor)	ckage)	PW DG	G = 8/14/16 G = 48/56/6	5/20/24/28 54 pins	
LCC (plastic leaded chip N = 20/28/44/52/68/84 pil		SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins	PAH PAG PM PN	= 52 pins = 64 pins = 64 pins = 80 pins	S S S		DG	SOP (thin volume of the volume	0/24/48/5	outline package 66 pins
= Now = Planned		SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins	PCA, P. PCB	Z = 100 pii = 120 pii				– refer to p kage descrip		



AHC

DEVICE	тов	NO. PINS	7 90827	FU	NCTION	981	JIM.	MIL	PDIP	SOIC	LABILITY SSOP	TSSOP	TVSOP	SOT	LITERATURI
SN74AHC573	10	20	Octal D-Ty	pe Trans	parent La	atch		V	V	~	V	V .	8	000	SCLS242E
SN74AHC574	nja.	20	Octal D-Ty	pe Flip-F	Гор			~	V	~	V	V	8	304	SCLS244B
SCL83158	10														
													14		
SGL8288G															

commercial package description and availability

PDIP (plastic dual-in-line package)

N = 14/16/20 pins NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now

+ = Planned

PH = 80 pins PQ = 100/132 pins

RC = 52 pins

SOIC (small-outline integrated circuit)

QFP (plastic quad flat package)

D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins PAH

PAG PM = 64 pins

PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package)

PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



AHCT

DEVICE	NO.	FUNCTION			AVAI	LABILITY				LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	SOT	REFERENCE
SN74AHCT1G00	5	Single 2-Input Positive-NAND Gate		ich	sarení Lai	panerT eq	rT-O late	20 0	V	SCLS316B
SN74AHCT1G04	5	Single Inverter Gate			go	P-qP-pq	otal D-Ty	20 0	+	SCLS319C
SN74AHCT1G08	5	Single 2-Input Positive-AND Gate							V	SCLS315B
SN74AHCT1G14	5	Single Schmitt-Trigger Inverter Gate							+	SCLS322C
SN74AHCT1G32	5	Single 2-Input Positive-OR Gate							V	SCLS320B
SN74AHCT1G86	5	Single 2-Input Exclusive-OR Gate					I mile		+	SCLS324B
SN74AHCT00	14	Quad 2-Input NAND Gate	V	~	V	~	V	+		SCLS229B
SN74AHCT02	14	Quad 2-Input NOR Gate		+	+	+	+			SCLS262C
SN74AHCT04	14	Hex Inverter	V	V	V	V	V	+		SCLS232D
SN74AHCT08	14	Quad 2-Input AND Gate	V	V	V	~	V			SCLS237B
SN74AHCT14	14	Hex Inverter With Schmitt Trigger	V	~	V	~	V			SCLS246D
SN74AHCT32	14	Quad 2-Input OR Gate	V	V	V	~	V	+		SCLS248B
SN74AHCT74	14	Dual D-Type Flip-Flop With Preset and Clear	~	~	V	V	V			SCLS263C
SN74AHCT86	14	Quad Exclusive-OR Gate	V	V	V	V	V			SCLS250C
SN74AHCT125	14	Quad Bus Buffer Gate (OE)	V	V	V	V	V			SCLS264D
SN74AHCT126	14	Quad Bus Buffer Gate (OE)	V	V	V	V	V			SCLS265E
SN74AHCT138	16	3-to-8 Decoder/Demultiplexer		+	+	+	+			SCLS266C
SN74AHCT139	16	Dual 2-to-4 Line Decoder/Demultiplexer		+	+	+	+			SCLS267D
SN74AHCT157	16	Quad 2-to-1 Data Selector/Multiplexer		+	+	+	+	H-I		SCLS347B
SN74AHCT158	16	Quad 2-to-1 Data Selector/Multiplexer		+	+	+	+			SCLS348B
SN74AHCT240	20	Octal Buffer/Driver	V	V	V	V	V			SCLS252B
SN74AHCT244	20	Octal Buffer/Driver	V	V	V	V	V	+		SCLS228C
SN74AHCT245	20	Octal Bus Transceiver	+	V	V	V	V	+		SCLS233C
SN74AHCT257	16	Quad 2-to-1 Data Selector/Multiplexer		+	+	+	+	THE		SCLS351A
SN74AHCT258	16	Quad 2-to-1 Data Selector/Multiplexer		+	+	+	+			SCLS344A
SN74AHCT373	20	Octal D-Type Transparent Latch	V	V	V	V	V			SCLS239D
SN74AHCT374	20	Octal D-Type Flip-Flop	V	V	V	V	V			SCLS241C
SN74AHCT540	20	Octal Buffer/Driver	V	V	V	V	V			SCLS268C
SN74AHCT541	20	Octal Buffer/Driver	V	V	V	V	V	97.17		SCLS269F
SN74AHCT573	20	Octal D-Type Transparent Latch	V	V	V	V	V			SCLS243E
SN74AHCT574	20	Octal D-Type Flip-Flop	V	V	V	V	V			SCLS245C
ommercial paci	kage de	escription and availability		gali	Helian	a bus n	oliako	and one	Menn	latinisanini
PDIP (plastic dual-in-line part = 14/16/20 pins NT = 24/28 pins NP = 28 pins		QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins	DBV =	(plastic thin	quad flat pa	ackage)	PV	V = 8/14/16 GG = 48/56/6	6/20/24/28 64 pins	ull-outline package pins
PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins		SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins	PAH PAG PM PN	= 52 pin = 64 pin = 64 pin = 80 pin	S S S	alivo-Enviro into environ sca suesen	DC	/SOP (thin vigit = 14/16/28B = 80/100	20/24/48/5	outline package) 66 pins
chedule / = Now h = Planned		SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins	PCA, P PCB	Z = 100 pi = 120 pi				L – refer to p		



ALB Advanced Low-Voltage BiCMOS

The specially designed 3.3-V ALB family uses the latest $0.6-\mu$ BiCMOS technology for bus-interface functions. In addition, ALB provides 25-mA drive at 3.3 V with maximum propagation delays of 2.2 ns, making it TI's fastest logic family to date. The inputs have clamping diodes to eliminate overshoot and undershoot.

The ALB family is currently available in a limited number of functions with Widebus™ and shrink-Widebus™ footprints with advanced packaging options such as shrink small-outline package (SSOP), thin shrink small-outline package (TVSOP), and planned for thin very small-outline package (TVSOP).

ALB

DEVICE	NO.		FUNCTION	1	VAILABILI	TY	LITERATURE
DEVICE	PINS		FUNCTION	SSOP	TSSOP	TVSOP	REFERENCE
SN74ALB16244	48	16-Bit Buffer/Driver		V	V	V	SCBS647A
SN74ALB16245	48	16-Bit Bus Transceiver		V	V	V	SCBS678

The specialty designed 3.3-V ALB family uses the latest 0.5-µ BiCMO: technology for bus-interface functions. In addition, ALB provides 25-mA driver.

nd undersnoot.

such as shrink small-outline package (SSOP), thin shrink small-outline package (TVSOP), and planned for thin very small-outline package (TVSOP).

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
NT = 24/28 pins
NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now

+ = Planned

QFP (plastic quad flat package) RC = 52 pins

PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH = 52 pins PAG = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)

PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins

DBB = 80/100 pins



ALS Advanced Low-Power Schottky Logic

The ALS family provides a full spectrum of over 130 bipolar logic functions.

This family, combined with the AS family, can be used to optimize systems through performance budgeting. By using AS in speed-critical paths and ALS where speed is less critical, designers can optimize speed and power performance.

The ALS family includes gates, flip-flops, counters, drivers, transceivers, registered transceivers, readback latches, clock drivers, register files, and multiplexers.

For ALS data sheets, see the 1995 ALS/AS Logic Data Book, literature number SDAD001C.

ALS

DEVICE	NO. PINS	FUNCTION	MIL	AVAIL	ABILITY	SSOP	LITERATURE REFERENCE
SN74ALS00A	14	Quad 2-Input Positive-NAND Gate	V	V	V		SDAS187A
SN74ALS02A	14	Quad 2-Input Positive-NOR Gate	V	V	V	THE	SDAS111B
SN74ALS03B	14	Quad 2-Input Positive-NAND Gate	V	V	V		SDAS013B
SN74ALS04B	14	Hex Inverter	V	V	V	V	SDAS063B
SN74ALS05A	14	Hex Inverter With Open-Collector Outputs	V	V	V	V	SDAS190A
SN74ALS08	14	Quad 2-Input Positive-AND Gate	V	V	V		SDAS191A
SN74ALS09	14	Quad 2-Input Positive-AND Gate With Open-Collector Outputs	V	V	V		SDAS084B
SN74ALS10A	14	Triple 3-Input Positive-NAND Gate	V	V	V		SDAS002B
SN74ALS11A	14	Triple 3-Input Positive-AND Gate	V	V	V		SDAS009C
SN74ALS20A	14	Dual 4-Input Positive-NAND Gate	V	V	V		SDAS192B
SN74ALS21A	14	Dual 4-Input Positive-AND Gate	V	V	V		SDAS085B
SN74ALS27A	14	Triple 3-Input Positive-NOR Gate	V	V	V		SDAS112B
SN74ALS30A	14	8-Input Positive-NAND Gate	V	V	V		SDAS010B
SN74ALS32	14	Quad 2-Input Positive-OR Gate	V	V	V	13:17	SDAS113B
SN74ALS35A	14	Hex Noninverter With Open-Collector Outputs		V	V		SDAS011C
SN74ALS37A	14	Quad 2-Input Positive-NAND Gate	V	V	V	To Be	SDAS195A
SN74ALS38B	14	Quad 2-Input Postive-NAND Gate With Open-Collector Outputs	V	V	V		SDAS196B
SN74ALS74A	14	Dual D-Type Flip-Flop With Clear and Preset	V	V	V		SDAS143C
SN74ALS86	14	Quad 2-Input Exclusive-OR Gate	V	V	V		SDAS006B
SN74ALS109A	16	Dual J-K Positive-Edge-Triggered Flip-Flop	V	V	~		SDAS198B
SN74ALS112A	16	Dual J-K Negative-Edge-Triggered Flip-Flop	V	V	V	19.17	SDAS199A
SN74ALS133	16	13-Input Positive-NAND Gate	V	V	V		SDAS202B
SN74ALS137A	16	3-to-8 Decoder/Demultiplexer With Address Registers	V	V	V		SDAS203C
SN74ALS138A	16	3-to-8 Decoder/Demultiplexer	V	V	V		SDAS055E
SN74ALS139	16	Dual 2-to-4 Decoder/Demultiplexer	V	V	V		SDAS204A
SN74ALS151	16	8-to-1 Data Selector/Multiplexer	V	V	V		SDAS205A
SN74ALS153	16	Dual 4-to-1 Data Selector/Multiplexer	V	V	V		SDAS206A
SN74ALS156	16	Dual 2-to-4 Decoder/Demultiplexer With Open-Collector Outputs	417	V	V		SDAS099C
SN74ALS157A	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	V		SDAS081C
SN74ALS158	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	~		SDAS081C
SN74ALS161B	16	4-Bit Synchronous Binary Counter	V	V	V		SDAS024A

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins PAH PAG PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ALS

DEVICE	NO. PINS	FUNCTION	MIL	AVAIL	ABILITY	SSOP	LITERATURE REFERENCE
SN74ALS163B	16	4-Bit Synchronous Binary Counter	V	V	10V 0	S A	SDAS024A
SN74ALS164A	14	8-Bit Parallel-Out Serial Shift Register	Rig-F	V	HOV 0	S A	SDAS159D
SN74ALS165	16	8-Bit Parallel-In Shift Register	V	V	NOV 0	2	SDAS157B
SN74ALS166	16	8-Bit Parallel-In Shift Register	187/10	V	100V 0	4 2	SDAS156C
SN74ALS169B	16	4-Bit Synchronous Up/Down Binary Counter	V	V	W 0	3	SDAS125B
SN74ALS174	16	Hex D-Type Flip-Flop With Clear	V	V	10V 0	1 2	SDAS207D
SN74ALS175	16	Quad D-Type Flip-Flop With Clear	V	18	8-10	9 1	SDAS207D
SN74ALS191A	16	4-Bit Synchronous Up/Down Binary Counter	V	V	00V 0	3 2	SDAS210C
SN74ALS193A	16	4-Bit Synchronous Up/Down Binary Counter With Dual Clock and Clear	V	V	OV O	3 2	SDAS211C
SN74ALS240A	20	Octal Buffer/Driver	V	V	0	S /	SDAS214C
SN74ALS240A-1	20	Octal Buffer/Driver	Layon	V	8 V 0	9 /	SDAS214C
SN74ALS241C	20	Octal Buffer/Driver	V	000	OV O	8 (SDAS153E
SN74ALS241C-1	20	Octal Buffer/Driver	1-qP	V	V	8 8	SDAS153E
SN74ALS243A	14	Quad Bus Transceiver	V	V	WW !	0 1	SDAS069B
SN74ALS244C	20	Octal Buffer/Driver	V	V	V	V	SDAS142C
SN74ALS244C-1	20	Octal Buffer/Driver	A-diR	V	V	8 /	SDAS142C
SN74ALS245A	20	Octal Bus Transceiver	V	V	V	V	SDAS272
SN74ALS245A-1	20	Octal Bus Transceiver	viecet.	V	W O	2 7	SDAS272
SN74ALS251	16	8-to-1 Data Selector/Multiplexer	V	V	V	2 /	SDAS215A
SN74ALS253	16	Dual 4-to-1 Data Selector/Multiplexer	V	V	WV O	2 14	SDAS216A
SN74ALS257A	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	W O	2 /	SDAS124C
SN74ALS258A	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	V	8 14	SDAS124C
SN74ALS259	16	8-Bit Addressable Latch	V	V	W C	2	SDAS217A
SN74ALS273	20	Octal D-Type Flip-Flop With Clear	V	V	V	9 8	SDAS218A
SN74ALS280	14	9-Bit Parity Generator/Checker	vlecan	V	V	s H	SDAS038C
SN74ALS299	20	8-Bit Universal Shift/Storage Register	V	V	OV O	2	SDAS220B
SN74ALS323	20	8-Bit Universal Shift/Storage Register	V	V	10V 0	2	SDAS267A
SN74ALS373A	20	Octal D-Type Transparent Latch	V	V	V O	V	SDAS083B
SN74ALS374A	20	Octal D-Type Flip-Flop	V	V	V	V	SDAS167B
SN74ALS520	20	8-Bit Identity Comparator	V	V	10V 0	9 1-	SDAS224B
SN74ALS521	20	8-Bit Identity Comparator	red Bu	V	V	2 1	SDAS224B

commercial package description and availability

PDIP (plastic dual-in-line package)

N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now - Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)

D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH = 52 pins = 64 pins PAG PM = 64 pins

PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ALS

DE1/10E	NO.	ENGALAVA		AVAIL	ABILITY		LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	REFERENCE
SN74ALS533A	20	Octal D-Type Transparent Latch	ous Binary Counter	V	8 1 8	r B	SDAS270
SN74ALS534A	20	Octal D-Type Flip-Flop	Serial Skift Regi	V	V	Y A	SDAS168B
SN74ALS540	20	Octal Buffer/Driver	nateigeR fil/f8	V	. V		SDAS025C
SN74ALS540-1	20	Octal Buffer/Driver	n Shift Register	~	-V		SDAS025C
SN74ALS541	20	Octal Buffer/Driver	N Up/Down Bings	V .	. V .	1 8	SDAS025C
SN74ALS541-1	20	Octal Buffer/Driver	p-Flog With Oldan	- V	xelV a		SDAS025C
SN74ALS561A	20	4-Bit Synchronous Binary Counter	N-Rop With Clear	00 V	V		SDAS125B
SN74ALS563B	20	Octal D-Type Transparent Latch	V UnDown Biner	V	. V .	1	SDAS163A
SN74ALS564B	20	Octal D-Type Flip-Flop	W Up/Down Blean	V 3	8 V 8	1 1	SDAS164B
SN74ALS568A	20	4-Bit Synchronous Up/Down Decade Counter	101/	V	doO 0	9	SDAS229A
SN74ALS569A	20	4-Bit Synchronous Up/Down Binary Counter	V	V	V	9 1-4	SDAS229A
SN74ALS573C	20	Octal D-Type Transparent Latch	V		V	V	SDAS048D
SN74ALS574B	20	Octal D-Type Flip-Flop	V	V	V	1-0	SDAS165B
SN74ALS575A	24	Octal D-Type Flip-Flop	tsviese		V		SDAS165B
SN74ALS576B	20	Octal D-Type Flip-Flop	V	V	V	9 0	SDAS065B
SN74ALS577A	24	Octal D-Type Flip-Flop	nev!	V	V	3 10	SDAS065B
SN74ALS580B	20	Octal D-Type Transparent Latch	V	V	V	2 7	SDAS048D
SN74ALS620A	20	Octal Bus Transceiver	navlage	V	0 V	3 1-7	SDAS226A
SN74ALS621A	20	Octal Bus Transceiver With Open-Collector Outputs	nexelatiful/fuctor	8 V	0 V 8		SDAS226A
SN74ALS621A-1	20	Octal Bus Transceiver With Open-Collector Outputs	celathuAfaotanta2 si	V	V	1	SDAS226A
SN74ALS623A	20	Octal Bus Transceiver	na Selector/Authola	01	3 V 8	1 /	SDAS226A
SN74ALS638A-1	20	Octal Bus Transceiver	na Šelector/Multiple	V	W a		SDAS123A
SN74ALS639A	20	Octal Bus Transceiver	date Latels	V	V		SDAS123A
SN74ALS640B	20	Octal Bus Transceiver	V ton With Clear	~	V	g	SDAS122A
SN74ALS640B-1	20	Octal Bus Transceiver	receionOnotare.	V	V	7-	SDAS122A
SN74ALS641A	20	Octal Bus Transceiver With Open-Collector Outputs	Shift/Storage Reck	V		9	SDAS300
SN74ALS641A-1	20	Octal Bus Transceiver With Open-Collector Outputs	Shift/Storage Regi	V	~		SDAS300
SN74ALS642A-1	20	Octal Bus Transceiver With Open-Collector Outputs	Adal Inggoras	V	50V 0	2 0	SDAS300
SN74ALS645A	20	Octal Bus Transceiver	~	V	V	9	SDAS278
SN74ALS645A-1	20	Octal Bus Transceiver	outparelor	V	8 V 0		SDAS278
SN74ALS646A	24	Octal Registered Bus Transceiver	V	V	V	9	SDAS039F

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

 = Now + = Planned QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)

D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package) PAH = 52 pins

= 52 pins = 64 pins = 64 pins PAG PM PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ALS

DEVICE	NO. PINS	FUNCTION MOTORIDA	MIL	AVAIL PDIP	ABILITY	SSOP	LITERATURE
SN74ALS646A-1	24	Octal Registered Bus Transceiver	rallhia:	V	OF VIE	9	SDAS039F
SN74ALS648A	24	Octal Registered Bus Transceiver	V	V	tell vitex	8	SDAS039F
SN74ALS651A	24	Octal Registered Bus Transceiver	uB gritn	~	TO V OT		SDAS066F
SN74ALS651A-1	24	Octal Registered Bus Transceiver	lu6 gnith	V	selv in	8	SDAS066F
SN74ALS652A	24	Octal Registered Bus Transceiver	V	V	20 VOOL	A	SDAS066F
SN74ALS652A-1	24	Octal Registered Bus Transceiver	evisoen	V	20. VOdi	Aa	SDAS066F
SN74ALS653	24	Octal Registered Bus Transceiver	V	V	100V 03	AG	SDAS066F
SN74ALS654	24	Octal Registered Bus Transceiver	aviecen	V	100V 08	- A8	SDAS066F
SN74ALS666	24	8-Bit D-Type Transparent Readback Latch	W revirl	V 1	20 400	0	SDAS227A
SN74ALS667	24	8-Bit D-Type Transparent Readback Latch	W revitt	V	20 VOOR		SDAS227A
SN74ALS688	20	8-Bit Identity Comparator	V	V	30 V 10	rs	SDAS228A
SN74ALS760	20	Octal Buffer/Driver With Open-Collector Outputs	Driver	V	26 40-6	75	SDAS141A
SN74ALS804A	20	Hex 2-Input NAND Gate	V	V	21 101	89	SDAS022C
SN74ALS805A	20	Hex 2-Input NOR Gate	V	V	8-8V 19	88	SDAS023C
SN74ALS832A	20	Hex 2-Input Positive-OR Gate	V	90	10 V 15	13	SDAS017C
SN74ALS841	24	10-Bit Bus-Interface D-Type Latch	nscelver	V	8 V 15	88	SDAS059C
SN74ALS842	24	10-Bit Bus-Interface D-Type Latch		V	V		SDAS059C
SN74ALS843	24	9-Bit Bus-Interface D-Type Latch		V	~		SDAS232A
SN74ALS845	24	8-Bit Bus-Interface D-Type Latch		V	~		SDAS233A
SN74ALS857	24	Hex 2-to-1 Universal Multiplexer	V	V	V		SDAS170A
SN74ALS867A	24	8-Bit Synchronous Up/Down Binary Counter		V	~		SDAS115C
SN74ALS869	24	8-Bit Synchronous Up/Down Binary Counter		V	V		SDAS115C
SN74ALS870	24	Dual 16 × 4 Register File	V	V	V		SDAS139A
SN74ALS873B	24	Dual 4-Bit D-Type Latch	V	V	V		SDAS036D
SN74ALS874B	24	Dual 4-Bit D-Type Edge-Triggered Flip-Flop	V	V	V		SDAS061C
SN74ALS876A	24	Dual 4-Bit D-Type Edge-Triggered Flip-Flop	John H	V	V		SDAS061C
SN74ALS990	20	8-Bit D-Type Transparent Readback Latch		V	V		SDAS027B
SN74ALS992	24	9-Bit D-Type Transparent Readback Latch		V	V		SDAS028B
SN74ALS994	24	10-Bit D-Type Transparent Readback Latch	5149	V	V		SDAS237A
SN74ALS996	24	8-Bit D-Type Edge-Triggered Readback Latch	V	V	~		SDAS098B
SN74ALS996-1	24	8-Bit D-Type Edge-Triggered Readback Latch		V	V		SDAS098B

commercial package description and availability

PDIP (plastic dual-in-line package)

N = 14/16/20 pins NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins
PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ALS

DEVICE	1101				FUNCTION				AVAIL	ABILIT	Y	LITERATUR
DEVICE	PINS	08 4	PDB	JIM	FUNCTION	HOTT	SHUH	MIL	PDIP	SOIC	SSOP	REFERENC
SN74ALS1004	14	Hex In	vertin	g Buffer			revisoureiT	sud box	V	OV	12 1-	SDAS074B
SN74ALS1005	14	Hex In	vertin	g Buffer With	Open-Collector Outp	outs	nevlacerenT	V	~	V	49	SDAS240A
SN74ALS1034	14	Hex N	oninve	erting Buffer			Transceiver	V	~	V	88	SDAS053B
SN74ALS1035	14	Hex N	oninve	erting Buffer \	With Open-Collector	Outputs	Transpelvar	V	V	1001	-1 24	SDAS243A
SN74ALS1244A	20	Octal I	Buffer/	Driver (Driver			reviecement	V	~	V	24	SDAS186B
SN74ALS1245A	20	Octal I	Bus Tr	ansceiver			Timpopiyar	V	V	OV	48 1-	SDAS245A
SN74ALS1640A	20	Octal I	Bus Tr	ansceiver			Transceiver	au8 box	V	100	24	SDAS246A
SN74ALS1645A	20	Octal I	Bus Tr	ansceiver			Transceiver	suß ben	V	V	24	SDAS246A
SN74ALS2240	20	Octal I	Buffer/	Driver With S	Series Resistors	rtofall :	rent Rasybad	egenerT	0 VO	V	18	SDAS268
SN74ALS2541	20	Octal I	Buffer/	Driver With S	Series Resistors	dotn.l.)	bacbach iner	sonnerT	W 01	30	85	SDAS273
SN74ALS29821	24	10-Bit	Bus-Ir	nterface Flip-	Flop		10/5	V	V	V	00	SDAS145B
SN74ALS29827	24	10-Bit	Buffer	/Driver		ator Output	ith Open Colle	W yawin0	V	V	20	SDAS095B
SN74ALS29828	24	10-Bit	Buffer	/Driver	FEET STATE		efa	& GHA	V	V	20	SDAS095B
SN74ALS29833	24	8-Bit to	9-Bit	Parity Bus T	ransceiver		9	se Aoi	~	V	02	SDAS119D
SN74ALS29841	24	10-Bit	D-Typ	e Bus-Interfa	ce Latch		els® RC	-avdino	V	V	20	SDAS149A
SN74ALS29863	24	9-Bit B	us Tra	ansceiver			riote.) eqyT-0	egahal	V	-014	AS.	SDAS096C
SDASOSSC		N	4				Type Latch	l soehul	ni-eu8 1/8	10-1	24	NYAALSSAZ

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned

QFP (plastic quad flat package) RC = 52 pins PH = 80 pins

PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package) PAH

= 52 pins = 64 pins PAG = 64 pins PM PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)

PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ALVC Advanced Low-Voltage CMOS Technology

One of the highest performance 3.3-V bus-interface families is the ALVC family. These specially designed 3-V products are processed in 0.6- μ CMOS technology, giving typical propagation delays less than 3 ns, along with current drive of 24 mA and static power consumption of 40 μ A for bus-interface functions. The ALVC devices have bus-hold cells on inputs to eliminate the need for external pullup resistors for floating inputs. The family also includes innovative functions for memory interleaving, multiplexing, and interfacing to synchronous DRAMs.

The ALVC family is offered in the Widebus™ footprints with all of the advanced packaging such as shrink small-outline package (SSOP) and thin shrink small-outline package (TSSOP).

For ALVC data sheets, see the 1996 Low-Voltage Logic Data Book, literature number SCBD003B, and the 1997 High-Speed Memory Interface Logic Data Book, literature number SCED001.

ALVC

DINON GUID	NO.	DEVICE	A	VAILABILIT	TY	LITERATURE
DEVICE	PINS	FUNCTION	SSOP	TSSOP	TVSOP	REFERENCE
SN74ALVC16244A	48	16-Bit Buffer/Driver	V	V		SCAS250E
SN74ALVC164245	48	16-Bit Transceiver and 3.3-V to 5-V Shifter	V	~		SCAS416A
SN74ALVCH16240	48	16-Bit Buffer/Driver	~	~		SCES045A
SN74ALVCH16241	48	16-Bit Buffer/Driver	+	+		Call
SN74ALVCH16244	48	16-Bit Buffer/Driver	V	~	+	SCES014
SN74ALVCH16245	48	16-Bit Bus Transceiver	~	~	V	SCES015
SN74ALVCH16260	56	12-to-24 Multiplexed D-Type Latch	V	V		SCES046
SN74ALVCH16268	56	12-to-24 Registered Bus Exchanger	+	+		Call
SN74ALVCH16269	56	12-to-24 Registered Bus Exchanger	V	V		SCES019/
SN74ALVCH16270	56	12-to-24 Registered Bus Exchanger	V	~		SCES028A
SN74ALVCH16271	56	12-to-24 Multiplexed Bus Exchanger	V	V		SCES017
SN74ALVCH16272	56	12-to-24 Multiplexed Bus Exchanger	+	+		SCES057/
SN74ALVCH16282	80	18-to-36 Registered Bus Exchanger			V	SCES036
SN74ALVCH16334	48	16-Bit Universal Bus Driver	+	+		SCES090
SN74ALVCH16344	56	1-to-4 Address Driver	V	~		SCES054I
SN74ALVCH16373	48	16-Bit D-Type Transparent Latch		V		SCES020/
SN74ALVCH16374	48	16-Bit D-Type Flip-Flop	V	V		SCES021/
SN74ALVCH16409	56	9-Bit, 4-Port Universal Bus Exchanger	V	V		SCES022/
SN74ALVCH16500	56	18-Bit Universal Bus Transceiver	V	~		SCES0230
SN74ALVCH16501	56	18-Bit Universal Bus Transceiver	~	V		SCES024/
SN74ALVCH16524	56	18-Bit Registered Bus Transceiver	V	~		SCES080
SN74ALVCH16525	56	18-Bit Registered Bus Transceiver	V	V		SCES059/
SN74ALVCH16540	48	16-Bit Buffer/Driver	+	+		SCES029
SN74ALVCH16541	48	16-Bit Buffer/Driver	+	+		SCES031
SN74ALVCH16543	56	16-Bit Registered Bus Transceiver	V	V		SCES025
SN74ALVCH16600	56	18-Bit Universal Bus Transceiver	V	~		SCES030/
SN74ALVCH16601	56	18-Bit Universal Bus Transceiver	V	V		SCES027/
SN74ALVCH16646	56	16-Bit Registered Bus Transceiver	~	V		SCES032/
SN74ALVCH16652	56	16-Bit Bus Transceiver and Register	+	+		SCES034
SN74ALVCH16721	56	20-Bit Bus-Interface Flip-Flop	V	V	+	SCES052/
SN74ALVCH16820	56	10-Bit Bus-Interface Flip-Flop	V	V	Maria II	SCES035/

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

= Now + = Planned QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)

D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins = 64 pins PAH PAG PM PN PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



ALVC

DEVICE	NO. PINS	FUNCTION		SSOP	VAILABILIT TSSOP	TVSOP	LITERATUR
SN74ALVCH16821	56	20-Bit Bus-Interface Flip-Flop	a Transparkus Willia Sarios	SSUP	135UP	+	SCES037
SN74ALVCH16823	56	18-Bit Bus-Interface Flip-Flop	Burkeland Sue Perhance	~	V	DROORES	SCES038
SN74ALVCH16825	56	18-Bit Buffer/Driver	Registered Bull Funkanea	~	V	CRCCR15	SCES039
SN74ALVCH16827	56	20-Bit Buffer/Driver	rug (Injuggool Eura Eveluge	~	V	0+31	SCES041
SN74ALVCH16830	80	1-to-2 Address Driver	THE PERSON NAMED IN COLUMN 2 INC.			+	SCES081
SN74ALVCH16831	80	1-to-4 Address Driver				+	SCES083
SN74ALVCH16835	56	18-Bit DFF Memory Buffer		V	V		SCES053
SN74ALVCH16836	56	20-Bit Universal Bus Driver		+	+		SCES089
SN74ALVCH16841	56	20-Bit Bus-Interface D-Type Latch		~	· ·		SCES043
SN74ALVCH16843	56	16-Bit Bus-Interface D-Type Latch		+	+		SCES044
SN74ALVCH16863	48	18-Bit Bus Transceiver		~	~		SCES060
SN74ALVCH16901	64	18-Bit Universal Bus Transceiver With Clock Er	nable Parity Generator		V		SCES010
SN74ALVCH16952	56	16-Bit Registered Bus Transceiver	lable, I ality deliciator	V	V		SCES011
SN74ALVCH162240	48	16-Bit Buffer/Driver With Series Resistors		+	+		Call
SN74ALVCH162244	48	16-Bit Buffer/Driver With Series Resistors		~	~	-	SCES065
SN74ALVCH162245	48	16-Bit Bus Transceiver With Series Resistors		+	+		Call
SN74ALVCH162260	56	12-to-24 Multiplexed D-Type Latch With Series	Resistors	~	~		SCAS570
SN74ALVCH162268	56	12-to-24 SDRAM Interleave Multiplexer With Series-Damping Resistors	Tiodiotoro	~	V		SCES018
SN74ALVCH162280	80	16-to-32 Registered Bus Exchanger				+	Call
SN74ALVCH162344	56	1-to-4 Address Driver With Series Resistors		~	V		SCES085
SN74ALVCH162373	48	16-Bit D-Type Transparent Latch With Series-D	amping Resistors	+	+		Call
SN74ALVCH162374	48	16-Bit D-Type Flip-Flop With Series-Damping F	Resistors	+	+		Call
SN74ALVCH162525	56	18-Bit Registered Bus Transceiver With Series-	-Damping Resistors	V	V		SCES058
SN74ALVCH162540	48	16-Bit Buffer/Driver With Series Resistors		+	+		Call
SN74ALVCH162601	56	18-Bit Universal Bus Transceiver With Series R	esistors	V	V	72.11	SCES026
SN74ALVCH162721	56	20-Bit Bus-Interface Flip-Flop		V	V		SCES055
SN74ALVCH162820	56	10-Bit Bus-Interface Flip-Flop With Dual Output	s	V	V		SCES012
SN74ALVCH162821	56	20-Bit Bus-Interface Flip-Flop With Series-Dam	ping Resistor	+	+		Call
SN74ALVCH162827	56	20-Bit Buffer/Driver With Series-Damping Resis	stors	V	V	+	SCES013
SN74ALVCH162830	80	1-to-2 Address Driver				V	SCES082
SN74ALVCH162831	80	1-to-4 Address Driver				+	SCES084
ommercial package	desc	eription and availability	will state best	nobel	torek er	padeag	Intoseann
DIP (plastic dual-in-line package = 14/16/20 pins T = 24/28 pins P = 28 pins	18 - 14 14 - 80 1 4084	RC = 52 pins DBV = PH = 80 pins	small-outline transistor) 5 pins (plastic thin quad flat package) = 52 pins	10) 990 20 - 38 30 - 19 30 - 19	PW = 8/14 DGG = 48/5	/16/20/24/28 6/64 pins	Il-outline packa
LCC (plastic leaded chip carrier N = 20/28/44/52/68/84 pins chedule)† = V01	SOIC (small-outline integrated circuit) PAG D = 8/14/16 pins PM DW = 16/20/24/28 pins PN PCA F PCA F	= 64 pins = 64 pins = 80 pins		DGV = 14/1 DBB = 80/1	6/20/24/48/5	
= Now = Planned		SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins	= 120 pins		MIL – refer t package des		



ALVC

DEVICE	NO.	FUNCTION		/AILABILIT	ΓY	LITERATURE
DEVICE	PINS	FUNCTION	SSOP	TSSOP	TVSOP	REFERENCE
SN74ALVCHR162245	48	16-Bit Bus Transceiver With Series Resistors	20-N Bus-Intertool Plo-Plop	V	1388	SCES064
SN74ALVCHR162269	56	12-to-24 Registered Bus Exchanger	10-N Bus Interfece Filip Flog.	V	-6988	SCES050A
SN74ALVCHR162282	80	18-to-36 Registered Bus Exchanger	revhChallo8 #8-61	88	+388	SCES087
SN74ALVCHR162409	56	9-Bit, 4-Port Universal Bus Exchanger With Series	Resistors	V	8827	SCES056A
r609308 4			1-to-2 Address Criver	08	6830	SHIMALVOHI

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins	QFP (plastic quad flat package) RC = 52 pins PH = 80 pins	SOT (small-outline transistor) DBV = 5 pins	TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins
NP = 28 pins	PQ = 100/132 pins	TQFP (plastic thin quad flat package)	and the latest and th
PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins	SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins	PAH = 52 pins PAG = 64 pins PM = 64 pins PN = 80 pins	TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins
schedule	2000 4111 # 100 918	PCA, PZ = 100 pins	
✓ = Now+ = Planned	SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins	PCB = 120 pins	MIL – refer to page 4–1 for military package description and availability



AS Advanced Schottky Logic

The AS family of high-performance bipolar logic includes over 90 functions that offer high drive capabilities.

This family, combined with the ALS family, can be used to optimize system speed and power through performance budgeting. By using AS in speed-critical paths and ALS where speed is less critical, designers can optimize speed and power performance.

The AS family includes gates, flip-flops, counters, drivers, transceivers, registered transceivers, readback latches, clock drivers, register files, and multiplexers.

For AS data sheets, see the 1995 ALS/AS Logic Data Book, literature number SDAD001C.

AS

DENCE NO	NO.	D. FUNCTION			ITY	LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	REFERENCE
SN74AS00	14	Quad 2-Input Positive-NAND Gate	~	V	V	SDAS187A
SN74AS02	14	Quad 2-Input Positive-NOR Gate	~	V	V	SDAS111B
SN74AS04	14	Hex Inverter	~	~	V	SDAS063B
SN74AS08	14	Quad 2-Input Positive-AND Gate	~	V	~	SDAS191A
SN74AS10	14	Triple 3-Input Positive-NAND Gate	~	~	V	SDAS002B
SN74AS11	16	Triple 3-Input Positive-AND Gate	V	V	V	SDAS009C
SN74AS20	14	Dual 4-Input Positive-NAND Gate	~	V	V	SDAS192B
SN74AS21	14	Dual 4-Input Positive-AND Gate		V	V	SDAS085B
SN74AS27	14	Triple 3-Input Positive-NOR Gate	V	V	V	SDAS112B
SN74AS30	14	8-Input Positive-NAND Gate	V	V	V	SDAS010B
SN74AS32	14	Quad 2-Input Positive-OR Gate	V	V	V	SDAS113B
SN74AS74A	14	Dual D-Type Flip-Flop	V	V	V	SDAS143C
SN74AS109A	16	Dual J-K Edge-Triggered Flip-Flop	~	V	V	SDAS198B
SN74AS137	16	3-to-8 Decoder/Demultiplexer		V	V	SDAS203C
SN74AS138	16	3-to-8 Decoder/Demultiplexer	~	V	V	SDAS055E
SN74AS151	16	8-to-1 Data Selector/Multiplexer		V	V	SDAS205A
SN74AS153	16	Dual 4-to-1 Data Selector/Multiplexer		V	V	SDAS206A
SN74AS157	16	Quad 2-to-1 Data Selector/Multiplexer		V	V	SDAS081C
SN74AS158	16	Quad 2-to-1 Data Selector/Multiplexer		V	V	SDAS081C
SN74AS161	16	4-Bit Synchronous Binary Counter	V	V	V	SDAS024A
SN74AS163	16	4-Bit Synchronous Binary Counter	V	V	V	SDAS024A
SN74AS169A	16	4-Bit Synchronous Up/Down Binary Counter	V	V	V	SDAS125B
SN74AS174	16	Hex D-Type Flip-Flop With Clear	V	V	V	SDAS207D
SN74AS175B	16	Quad D-Type Flip-Flop With Clear	V	V	V	SDAS207D
SN74AS181A	24	4-Bit Arithmetic Logic Unit	~	V	V	SDAS093A
SN74AS194	16	4-Bit Bidirectional Universal Shift Register	~	V	V	SDAS212A
SN74AS230A	14	Octal Buffer/Driver		V	V	SDAS213B
SN74AS240A	20	Octal Buffer/Driver	V	V	V	SDAS214C
SN74AS241A	20	Octal Buffer/Driver	~	V	V	SDAS153E
SN74AS244A	20	Octal Buffer/Driver	V	V	V	SDAS142C
SN74AS245	20	Octal Bus Transceiver	V	V	V	SDAS272

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
NT = 24/28 pins
NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now

+ = Planned

QFP (plastic quad flat package) RC = 52 pins

PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)

D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH PAG = 52 pins = 64 pins = 64 pins PM PN PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



DEVICE	NO.	IAJAVA		1	AVAILABILIT		LITERATURE
DEVICE	PINS	FUNCTIO	N MORGAN	MIL	PDIP	SOIC	REFERENCE
SN74AS250A	20	16-to-1 Data Generator/Multiplexer	tertapa Rip-Flop	V	SV	2 1	SDAS137A
SN74AS253A	16	Dual 4-to-1 Data Selector/Multiplexer	eta D RO	tuqni-S	V	SV	SDAS216A
SN74AS257	16	Quad 2-to-1 Data Selector/Multiplexer	roncus Up/Down Binery Counter	Synch	V	SV	SDAS124C
SN74AS258	16	Quad 2-to-1 Data Selector/Multiplexer	ranous UpiDown Binary Courtier	Synch	V	s v	SDAS124C
SN74AS280	14	9-Bit Parity Generator/Checker	-1\pa Flp-Flop	118-4	V	8 1	SDAS038C
SN74AS286	14	9-Bit Parity Generator/Checker	GoR-oiR bereggint-egb3 egyT-C	V	SV	8 4	SDAS050B
SN74AS298A	16	Quad 2-to-1 Multiplexer	Type Edge-Triggered Filp-Ficp	1,614	NV I	8 4	SDAS219B
SN74AS353B	16	Dual 4-to-1 Data Selector/Multiplexer	lude Comparator	Magni	18 V	V	SDAS222A
SN74AS373	20	Octal D-Type Transparent Latch	els© CMAI4-evilise Tit	V	V	1	SDAS083B
SN74AS374	20	Octal D-Type Flip-Flop	ng Puling	V	XIV I	~	SDAS167B
SN74AS533A	20	Octal D-Type Transparent Latch	ut Positive-AND Gate	oni-Si	V	1	SDAS254A
SN74AS573A	20	Octal D-Type Transparent Latch	arta Provide OR Gara	V	V	10	SDAS048D
SN74AS574	20	Octal D-Type Flip-Flop	erling Buller	V	xelV	1	SDAS165B
SN74AS575	24	Octal D-Type Flip-Flop	MAND Gala	V	XV C	SV	SDAS165B
SN74AS576	20	Octal D-Type Flip-Flop	NOR Gale	V	xelV (3 V	SDAS065B
SN74AS639	20	Octal Bus Transceiver	e Positive AND Gate	ugrit-s	VV C	8 1	SDAS123A
SN74AS640	20	Octal Bus Transceiver	AlpD RO-extisoR1	V	NV (V	SDAS122A
SN74AS641	20	Octal Bus Transceiver	Fank Synchronizer	Hauti	NV O	SV	SDAS300
SN74AS645	20	Octal Bus Transceiver		V	V	V	SDAS278
SN74AS646	24	Octal Registered Bus Transceiver		V	V	V	SDAS039F
SN74AS648	24	Octal Registered Bus Transceiver			V	V	SDAS039F
SN74AS651	24	Octal Registered Bus Transceiver		V	V	V	SDAS066F
SN74AS652	24	Octal Registered Bus Transceiver		V	V	V	SDAS066F
SN74AS756	20	Octal Buffer/Driver		~	V	V	SDAS040B
SN74AS757	20	Octal Buffer/Driver		THE	V	V	SDAS040B
SN74AS760	20	Octal Buffer/Driver		V	V	V	SDAS141A
SN74AS804B	20	Hex 2-Input NAND Gate		V	V	V	SDAS022C
SN74AS805B	20	Hex 2-Input NOR Gate		V	V	V	SDAS023C
SN74AS808B	20	Hex 2-Input Positive-AND Gate		V	V	V	SDAS018C
SN74AS821A	24	10-Bit Bus-Interface Flip-Flop		V	V	V	SDAS230A
SN74AS823A	24	9-Bit Bus-Interface Flip-Flop		V	V	V	SDAS231A

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package) PAH

= 52 pins = 64 pins PAG PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



AS

DEVICE		NO.	FUNCTION 150 TO			VAILABIL	LITERATURE	
DEVICE	010	PINS	PONCTION IN	11000	MIL	PDIP	SOIC	REFERENCE
SN74AS825A	10	24	8-Bit Bus-Interface Flip-Flop	Generation Multiplexer	· V	181	9 1	SDAS020B
SN74AS832B	N	20	Hex 2-Input OR Gate	Jata Selector/Multiplexer	~	SUV I	1	SDAS017C
SN74AS867	N	24	8-Bit Synchronous Up/Down Binary Counter	Data Selector/Multiplaxer	V	V	~	SDAS115C
SN74AS869	1	24	8-Bit Synchronous Up/Down Binary Counter	Ogta Selectorikuttiplexer	1 W	sul v	V.	SDAS115C
SN74AS873A	30	24	Dual 4-Bit D-Type Flip-Flop	renerator/Chaoker	V	8 V	1	SDAS036D
SN74AS874	N	24	Dual 4-Bit D-Type Edge-Triggered Flip-Flop	Seneralor/Checker	V	V	· ·	SDAS061C
SN74AS876	N	24	Dual 4-Bit D-Type Edge-Triggered Flip-Flop	hexelqitleM	f-e3-S b	SIV 8	V	SDAS061C
SN74AS885	No	24	8-Bit Magnitude Comparator	Sate Selector/Multiplexer	V	sulV 8	1	SDAS236A
SN74AS1000A	M	14	Quad 2-Input Positive-NAND Gate	Transparent Latch	V	W C	3 4	SDAS056B
SN74AS1004A	N	14	Hex Inverting Buffer	goPl-qiPl	V	OV C	V	SDAS074B
SN74AS1008A	N	14	Quad 2-Input Positive-AND Gate	Transparent Latels	oy(T-Q le	V	9 1	SDAS071B
SN74AS1032A	N	14	Quad 2-Input Positive-OR Gate	riotal transgenerif e	V	V	5 V	SDAS072B
SN74AS1034A	10	14	Hex Noninverting Buffer	Pip-Rop	V	V	2 1	SDAS053B
SN74AS1804	No	20	Hex 2-Input NAND Gate	poR-qIP	gyT-Q la	V	g.	SDAS042C
SN74AS1805	V	20	Hex 2-Input NOR Gate	gpR-glPl	i D-Tygs	V	2	SDAS043C
SN74AS1808	10	20	Hex 2-Input Positive-AND Gate	ngvinoens	of eu8 to	V	9	SDAS044C
SN74AS1832	10	20	Hex 2-Input Positive-OR Gate	nevieren	Tavê k	V	2	SDAS045C
SN74AS4374B	1	20	8-Bit Dual-Rank Synchronizer	reviewer	T au8 b	V	SV	SDAS109D
SDA3278	10		V V	hovikoana	T au8 h	odeo o	2	ANARAL TIAS

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins

PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)

DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins PM = 64 pins = 80 pins PN

PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 plns
DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins



BCT BiCMOS Bus-Interface Technology

BCT is a family of 8-, 9-, and 10-bit drivers, latches, transceivers, and registered transceivers. Designed specifically for bus-interface applications, BCT offers TTL I/O with high speeds, 64-mA output drive, and very low power in the disabled mode. Over 50 BCT functions are in production now.

A family of fast, high-drive bus-interface functions that provides the incident-wave switching required by large backplane applications has been incorporated into the BCT offering. Designed specifically to ensure incident-wave switching down to 25 Ω , the devices in the BiCMOS low-impedance driver family can maximize the speed and reliability of heavily loaded systems. Each device in this series delivers 188 mA of I_{OL} drive current.

Also included in our BCT family is a series of memory drivers. These devices incorporate a series-damping resistor to reduce overshoot and undershoot that can occur in memory-driving applications.

For BCT data sheets, see the 1994 BCT BiCMOS Bus-Interface Logic Data Book, literature number SCBD001B.

BCT

DEVICE	NO. PINS	FUNCTION	MIL	AVAIL	ABILITY	SSOP	LITERATURE
SN74BCT125A	14	Quad Bus Buffer Gate (OE)	V	V	V	-	SCBS032E
SN74BCT126A	14	Quad Bus Buffer Gate (OE)	V	V	V		SCBS252A
SN74BCT240	20	Octal Buffer/Driver	V	V	V	V	SCBS004E
SN74BCT241	20	Octal Buffer/Driver	MARKET V	V	V	V	SCBS005D
SN74BCT244	20	Octal Buffer/Driver	V	V	V	V	SCBS006E
SN74BCT245	20	Octal Bus Transceiver	018 v	V	V	V	SCBS013F
SN74BCT373	20	Octal D-Type Transparent Latch	V	V	V	V	SCBS016C
SN74BCT374	20	Octal D-Type Flip-Flop	V	V	V	V	SCBS019B
SN74BCT540A	20	Octal Buffer/Driver	V	V	V		SCBS012D
SN74BCT541A	20	Octal Buffer/Driver	V	V	V		SCBS011D
SN74BCT543	24	Octal Registered Bus Transceiver	V	V	V		SCBS026C
SN74BCT574	20	Octal D-Type Flip-Flop	NO TON			V	SCBS074B
SN74BCT623	20	Octal Bus Transceiver	V	~	V		SCBS020A
SN74BCT640	20	Octal Bus Transceiver	Amst A V	~	V		SCBS025C
SN74BCT646	24	Octal Registered Bus Transceiver	inebioni V	V	V		SCBS037C
SN74BCT652	24	Octal Registered Bus Transceiver	V incorpor	V	V		SCBS038A
SN74BCT756	20	Octal Buffer/Driver	-inebioni	V	V		SCBS056A
SN74BCT760	20	Octal Buffer/Driver	v low-impe	V	V		SCBS034B
SN74BCT2240	20	Octal Buffer/Driver With Series Resistors	V loaded ✓	V	V	V	SCBS030D
SN74BCT2244	20	Octal Buffer/Driver With Series Resistors	uo evinb 🗸	V	V		SCBS017C
SN74BCT2245	20	Octal Bus Transceiver With Series Resistors		V	V	V	SCBS102B
SN74BCT2827C	24	10-Bit Buffer/Driver With Series Resistors	UNIONA V	V	V		SCBS007E
SN74BCT2828B	24	10-Bit Buffer/Driver With Series Resistors	V	V	V		SCBS058A
SN74BCT2953	24	Octal Bus Registered Transceiver	TIBU JAKU	V	V		SCBS105B
SN74BCT25245	24	25-Ω Octal Bus Transceiver	rog wa	V	V		SCBS053B
SN74BCT29821	24	10-Bit Bus-Interface Flip-Flop	El standi	V	V		SCBS021D
SN74BCT29823	24	9-Bit Bus-Interface Flip-Flop		V	V		SCBS018D
SN74BCT29827B	24	10-Bit Buffer/Driver		V	V		SCBS008C
SN74BCT29834	24	8-to-9-Bit Parity Bus Transceiver		V	V		SCBS256
SN74BCT29841	24	10-Bit Bus-Interface D-Type Latch		V	V		SCBS024C
SN74BCT29843	24	9-Bit Bus-Interface D-Type Latch		V	V		SCBS022C

commercial package description and availability

PDIP (plastic dual-in-line package)

N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

= Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH PAG = 52 pins = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



BCT

	DEVICE	NO.	PUNAMAN		AVAIL	ABILITY		LITERATURE
D		PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	REFERENCE
SN74E	BCT29854	24	8-to-9-Bit Parity Bus Transceiver		V	V		SCBS257
SN74E	3CT29863B	24	9-Bit Bus Transceiver		V	V		SCBS015D

commercial package description and availability

PDIP (plastic dual-in-line package) QFP (plastic quad flat package) SOT (small-outline transistor) TSSOP (thin shrink small-outline package) N = 14/16/20 pins NT = 24/28 pins RC = 52 pins PH = 80 pins PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins DBV = 5 pins TQFP (plastic thin quad flat package) NP = 28 pins PQ = 100/132 pins TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins = 52 pins = 64 pins PAH PLCC (plastic leaded chip carrier) SOIC (small-outline integrated circuit) PAG D = 8/14/16 pins DW = 16/20/24/28 pins FN = 20/28/44/52/68/84 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins schedule SSOP (shrink small-outline package) ✓ = Now DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins MIL – refer to page 4–1 for military package description and availability + = Planned



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		FUNCTION			
SCREETED					

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PDIP systems dust-in-line pushings)
N = (4/16/20 pins)
NT = 24/26 pins
NP = 28 pins
NP = 28 pins

PECO (plusto inadet ohio cardo FII = 20/30 AVEDDRIPS pira

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980P (minita amatik-matina prading 26 = 140 (minita broketopie) sina

PN PCA

194 - 6 pha 194 - 6 pha 1947 (plants thin quad for padalg)

PAH = 52 pms PMG = 84 pms

PN = 80 ptos PCA, PZ = 190 pto PCS = 160 pto

PW = 8/14/16/2004/29 pins DDO = 68/66/24 pins TYPEON man soon mode, culture continues

TYBUP (Bis vely miss-DSV = FATREOCKAMS) DSB = 80/100 pins

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64BCT 64-Series BiCMOS Technology

The 64BCT family offers all the features found in TI's standard BCT family. In addition, the family is specified from –40°C to 85°C and incorporates circuitry to protect the device in live-insertion applications.

For 64BCT data sheets, see the 1994 BCT BiCMOS Bus-Interface Logic Data Book, literature number SCBD001B.

64BCT

DEVICE	NO.	FUNCTION	AVAILA	BILITY	LITERATURE
DEVICE	PINS	FUNCTION	PDIP	SOIC	
SN64BCT125A	14	Quad Bus Buffer Gate (OE)	V	V	SCBS052B
SN64BCT126A	14	Quad Bus Buffer Gate (OE)	V	V	SCBS051B
SN64BCT240	20	Octal Buffer/Driver	V	V	SCBS049A
SN64BCT241	20	Octal Buffer/Driver	V	V	SCBS046B
SN64BCT244	20	Octal Buffer/Driver	V	V	SCBS027A
SN64BCT245	20	Octal Bus Transceiver	V	V	SCBS040A
SN64BCT306	8	2-Bit Buffer/Driver	V	~	SCBS048B
SN64BCT541A	20	Octal Buffer/Line Driver	V	V	SCBS031B
SN64BCT757	20	Octal Buffer/Driver	V	~	SCBS479
SN64BCT25244	24	25-Ω Octal Buffer/Driver		V	SCBS477
SN64BCT25245	24	25-Ω Octal Bus Transceiver	V	V	SCBS060A
SN64BCT29828B	24	10-Bit Buffer/Driver	V	V	SCBS478

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
NT = 24/28 pins
NP = 28 pins QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins SOT (small-outline transistor) DBV = 5 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins PAH = 52 pins
PAG = 64 pins
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins
PCB = 120 pins TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins schedule SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins = Now MIL - refer to page 4-1 for military + = Planned DL = 28/48/56 pins package description and availability



BTA Bus-Termination Arrays

The BTA family from TI offers a space-saving, efficient, and effective solution to bus-termination requirements. In high-speed digital systems with long transmission lines, reflecting waves on the line can cause voltage undershoots and overshoots that lead to malfunctions at the driven input. A BTA is a series of diodes that clamps a signal on a bus or any other signal trace using high-frequency logic to eliminate overshoot and undershoot problems.

For BTA data sheets, see the 1994 *F Logic Data Book*, literature number SDFD001B, or contact the Product Information Center at (972) 644-5580.

BTA

DEVICE	NO.	PUNCTON	AVAILA	LITERATURE	
DEVICE	PINS	FUNCTION	PDIP	SOIC	REFERENCE
SN74ACT1071	16	10-Bit Bus-Termination Array		V	SCAS192
SN74ACT1073	20	16-Bit Bus-Termination Array		V	SCAS193
SN74F1016	20	16-Bit Schottky Barrier Diode R-C Bus-Termination Array		V	SDFS093G
SN74F1018	24	18-Bit Schottky Barrier Diode R-C Bus-Termination Array		V	SDFS094
SN74F1056	16	8-Bit Schottky Barrier Diode Bus-Termination Array		V	SDFS085
SN74S1050	16	12-Bit Schottky Barrier Diode Bus-Termination Array	V	~	SDLS015A
SN74S1051	16	12-Bit Schottky Barrier Diode Bus-Termination Array	V	~	Call
SN74S1052	20	16-Bit Schottky Barrier Diode Bus-Termination Array	V	V	SDLS016A
SN74S1053	20	16-Bit Schottky Barrier Diode Bus-Termination Array	V	V	SDLS017
SN74S1056	16	8-Bit Schottky Barrier Diode Bus-Termination Array		V	SDLS019A

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins	QFP (plastic quad flat package) RC = 52 pins PH = 80 pins	SOT (small-outline transistor) DBV = 5 pins TQFP (plastic thin quad flat package)	TSSOP (thin shrink small-outline package PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins
NP = 28 pins PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins	PQ = 100/132 pins SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins	PAH = 52 pins PAG = 64 pins PM = 64 pins PN = 80 pins	TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins
v = Now t = Planned	SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins	PCA, PZ = 100 pins PCB = 120 pins	MIL – refer to page 4–1 for military package description and availability



BTL/FB+ Backplane Transceiver Logic

The FB series devices are used for high-speed bus applications and are fully compatible with the IEEE 1194.1-1991 (BTL) and IEEE 896-1991 (Futurebus+) standards. These transceivers are available in 7-, 8-, 9-, and 18-bit versions with TTL and BTL translation in lower than 5-ns performance. Other features include drive up to 100 mA and bias pins for live-insertion applications.

For BTL/FB+ data sheets, see the 1997 *GTL*, *BTL*, and *ETL* Logic Data Book, literature number SCED004.

BTL/FB+

DEVICE	NO.	FUNCTION	A	LITERATURE		
DEVICE	PINS	FUNCTION	MIL	QFP	TQFP	REFERENCE
SN74FB1650	100	18-Bit TTL/BTL Universal Storage Transceiver			~	SCBS178H
SN74FB1651	100	17-Bit TTL/BTL Universal Storage Transceiver With Buffered Clock Lines			V	SCBS177H
SN74FB2031	52	9-Bit TTL/BTL Address/Data Transceiver	~	V		SCBS176G
SN74FB2032	52	9-Bit TTL/BTL Competition Transceiver	V	V		SCBS175E
SN74FB2033A	52	8-Bit TTL/BTL Registered Transceiver	V	V		SCBS174G
SN74FB2040	52	8-Bit TTL/BTL Transceiver	V	V		SCBS173F
SN74FB2041A	52	7-Bit TTL/BTL Transceiver		V		SCBS172E

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins	QFP (plastic quad flat package) RC = 52 pins	SOT (small-outline transistor) DBV = 5 pins	TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins
NT = 24/28 pins	PH = 80 pins	TQFP (plastic thin quad flat package)	DGG = 48/56/64 pins
NP = 28 pins	PQ = 100/132 pins	PAH = 52 pins	TVSOP (thin very small-outline package)
PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins	SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins	PAG = 64 pins PM = 64 pins PN = 80 pins	DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins
schedule		PCA, PZ = 100 pins	
✓ = Now	SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins	PCB = 120 pins	MIL - refer to page 4-1 for military
+ = Planned	DL = 28/48/56 pins		package description and availability



CBT Crossbar Technology

In today's computing market, power and speed are two of the main concerns. CBT can address both of these issues in bus-interface applications. CBT enables a bus-interface device to function as a very fast bus switch, effectively isolating buses when the switch is closed and offering very little propagation delay when the switch is open. These devices can function as high-speed bus interfaces between computer-system components such as the central processing unit (CPU) and memory. CBT devices also can be used as 5-V to 3.3-V translators, allowing designers to mix 5-V or 3.3-V components in the same system.

The CBT devices are available in advanced packaging such as shrink small-outline packages (SSOP) and thin shrink small-outline packages (TSSOP) for reduced board area.

For CBT data sheets, see the 1996 *CBT Bus Switches Crossbar Technology Data Book*, literature number SCDD001A.

CBT

WHEN MON	NO.	ing solvag			AVAILABI	LITY		LITERATURE
DEVICE	PINS	FUNCTION	MIL	SOIC	SSOP	TSSOP	TVSOP	REFERENCE
SN74CBT3125	14	Quad Bus Switch		~	V	V		SCDS021B
SN74CBT3126	14	Quad Bus Switch		+	+	+		SCDS020B
SN74CBT3244	20	Dual 4-Bit Bus Switch With '244 Pinout		~	~	~		SCDS001E
SN74CBT3245A	20	8-Bit Bus Switch With '245 Pinout	SHE	V	~	V	+	SCDS002G
SN74CBT3251	16	8-to-1 Multiplexer/Data Selector	45.00	+	+	+		SCDS019C
SN74CBT3253	16	Dual 4-Bit to 1-Bit FET Multiplexer/Demultiplexer	ori	2	~	~	+	SCDS018E
SN74CBT3257	16	Quad 2-to-1 Bit FET Multiplexer/Demultiplexer		~	~	V		SCDS017D
SN74CBT3306	8	Dual Bus Switch	today	1		~		SCDS016C
SN74CBTD3306	8	Dual Bus Switch With Level Shifting	so 18	0		V		SCDS030D
SN74CBTS3306	8	Dual Bus Switch With Clamping Diodes	eeldar	~		~		SCDS029B
SN74CBT3345	20	8-Bit Bus Switch	oletiny	V	V	V		SCDS027B
SN74CBT3383	24	10-Bit Bus-Exchange Switch	V	V	~	V		SCDS003F
SN74CBTH3383	24	10-Bit Bus-Exchange Switch With Bus Hold	ogne)	+	+	+		SCDS023E
SN74CBT3384A	24	10-Bit Bus Switch	25000	V	~	V	+	SCDS004F
SN74CBTD3384	24	10-Bit Bus Switch With Level Shifting	+	V	V	V	+	SCDS025F
SN74CBTS3384	24	10-Bit Bus Switch With Clamping Diodes	e ean	V	~	V		SCDS024D
SN74CBT3386	24	10-Bit Bus-Exchange Switch With Extended Voltage Range	27) es	+	+	+		SCDS022D
SN74CBT6800	24	10-Bit Bus Switch With Precharged Outputs for Live Insertion	o-lian	18 /	~	V		SCDS005G
SN74CBT16209	48	18-Bit Bus-Exchange Switch	V	1)	V	V	+	SCDS006G
SN74CBT16211	56	24-Bit Bus-Exchange Switch	ROW	a l	~	V	+	SCDS028D
SN74CBT16212	56	24-Bit Bus-Exchange Switch	S nis	n	V	V	+	SCDS007H
SN74CBT16213	56	24-Bit Bus-Exchange Switch			V	V		SCDS026D
SN74CBT16214	56	12-Bit 3-to-1 Bus-Select Switch			V	V		SCDS008G
SN74CBT16232	56	16-Bit to 32-Bit Synchronous FET Multiplexer	Jun 1		V	~		SCDS009F
SN74CBT16233	56	16-Bit to 32-Bit FET Multiplexer/Demultiplexer			V	V		SCDS010D
SN74CBT16244	48	16-Bit Bus Switch			+	+	+	SCDS031C

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
NT = 24/28 pins
NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins

PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)

PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



74F Fast Logic

74F logic is a general-purpose family of high-speed advanced bipolar logic. TI provides over 60 functions, including gates, buffer/drivers, bus transceivers, flip-flops, latches, counters, multiplexers, and demultiplexers in the 74F logic family.

For 74F data sheets, see the 1994 F Logic Data Book, literature number SDFD001B.

74F

DEVICE	NO.	FUNCTION		AVAIL	ABILITY		LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	REFERENCE
SN74F00	14	Quad 2-Input Positive-NAND Gate	~	V	V		SDFS035A
SN74F02	14	Quad 2-Input Positive-NOR Gate	V	~	~		SDFS036A
SN74F04	14	Hex Inverter	~	V	V		SDFS037A
SN74F08	14	Quad 2-Input Positive-AND Gate		V	~		SDFS038A
SN74F10	14	Triple 3-Input Positive-NAND Gate	~	~	~	10.8	SDFS039A
SN74F11	14	Triple 3-Input Positive-AND Gate	~	V	V		SDFS040A
SN74F20	14	Dual 4-Input Positive-NAND Gate	V	V	V		SDFS041A
SN74F21	be1416	Dual 4-Input Positive-AND Gate	~	V	V		SDFS006A
SN74F27	14	Triple 3-Input Positive-NOR Gate	V	V	V		SDFS042A
SN74F30	14	8-Input Positive-NAND Gate	V	V	V		SDFS043A
SN74F32	14	Quad 2-Input Positive-OR Gate	V	V	V		SDFS044A
SN74F38	14	Quad 2-Input Positive-NAND Gate	V	V	V		SDFS013A
SN74F74	14	Dual D-Type Flip-Flop	V	V	V		SDFS046A
SN74F86	14	Quad 2-Input Exclusive-OR Gate		V	V		SDFS019A
SN74F109	16	Dual J-K Positive-Edge-Triggered Flip-Flop With Clear and Preset	~	V	~		SDFS047A
SN74F112	14	Dual J-K Negative-Edge-Triggered Flip-Flop With Clear and Preset		V	~		SDFS048A
SN74F125	14	Quad Bus Buffer Gate (OE)		V .	~		SDFS016A
SN74F126	14	Quad Bus Buffer Gate (OE)		V	V		SDFS017A
SN74F138	16	3-to-8 Decoder/Demultiplexer	~	V	V		SDFS051B
SN74F151B	16	8-to-1 Data Selector/Multiplexer	V	V	V		SDFS023A
SN74F153	16	Dual 4-to-1 Data Selector/Multiplexer	V	~	V		SDFS052A
SN74F157A	16	Quad 2-to-1 Data Selector/Multiplexer	V	V .	V		SDFS053A
SN74F158A	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	V		SDFS054A
SN74F161A	16	4-Bit Synchronous Binary Counter		V	V		SDFS056A
SN74F163A	16	4-Bit Synchronous Binary Counter		V	V		SDFS088
SN74F169	16	4-Bit Synchronous Up/Down Binary Counter		V	V		SDFS089
SN74F174A	16	Hex D-Type Flip-Flop With Clear		V	V		SDFS029B
SN74F175	16	Quad D-Type Flip-Flop With Clear	V	V	V		SDFS058A
SN74F240	20	Octal Buffer/Driver	V	V	V	V	SDFS061A
SN74F241	20	Octal Buffer/Driver	V	V	V		SDFS090
SN74F243	14	Quad Bus Transceiver		V	V		SDFS086

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins

PAG = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins



DE1/10E	NO.	FINATION		AVAIL	ABILITY		LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	REFERENCE
SN74F244	20	Octal Buffer/Driver	V	V	V	~	SDFS063A
SN74F245	20	Octal Bus Transceiver	V	V	V	V	SDFS010A
SN74F251B	16	8-to-1 Data Selector/Multiplexer	~	~	~		SDFS066A
SN74F253	16	Dual 4-to-1 Data Selector/Multiplexer	V	V	V		SDFS064A
SN74F257	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	V		SDFS065A
SN74F258	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	V		SDFS067A
SN74F260	14	Dual 5-Input Positive-NOR Gate		V	V		SDFS012A
SN74F280B	14	9-Bit Parity Generator/Checker	V	V	V		SDFS008A
SN74F283	16	4-Bit Binary Full Adder With Fast Carry	V	V	V		SDFS069A
SN74F299	20	8-Bit Universal Shift/Storage Register	V	V	V	2 10	SDFS071A
SN74F373	20	Octal D-Type Transparent Latch	V	V	V	V	SDFS076A
SN74F374	20	Octal D-Type Flip-Flop	V	V	V	V	SDFS077A
SN74F377A	20	Octal D-Type Flip-Flop With Clock Enable		V	V		SDFS018D
SN74F521	20	8-Bit Identity Comparator	V	V	V		SDFS091
SN74F541	20	Octal Buffer/Driver	V	V	V		SDFS021A
SN74F543	24	Octal Registered Bus Transceiver		V	V	V	SDFS025B
SN74F573	20	Octal D-Type Transparent Latch	~	~	V		SDFS011A
SN74F574	20	Octal D-Type Flip-Flop		V	V		SDFS005A
SN74F623	20	Octal Bus Transceiver	~	~	V		SDFS087
SN74F2244	20	Octal Buffer/Driver With Series Resistors	TECH ON	~	V	V	SDFS095B
SN74F2245	20	Octal Bus Transceiver With Series-Damping Resistors		~	V		SDFS099
SN74F2373	20	Octal D-Type Transparent Latch With Series Resistors	tereste tur	V	V		SDFS100

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

= Now

+ = Planned

QFP (plastic quad flat package)
RC = 52 pins
PH = 80 pins
PQ = 100/132 pins

SOIC (small-outline integrated circuit)

D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

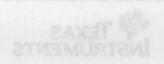
PAH = 52 pins
PAG = 64 pins
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins
PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



			14	
	4-Bit Binary Full Addar With Fast Carry			



FIFO First-In, First-Out Memories

TI has an extended product offering of Advanced CMOS (ACT) and Advanced BiCMOS (ABT) FIFOs. The FIFO product family includes clocked unidirectional and bidirectional FIFOs offered in 64K to 8K memory depths and 1-bit to 36-bit widths. Strobed unidirectional and bidirectional FIFOs are offered in 16K to 4K memory depths and 4-bit to 18-bit widths.

TI's application-specific FIFOs are specially designed for use in telecommunications, DSP, internetworking systems, and high-bandwidth computing. These devices include features such as parity generate and check, retransmit, bus matching, byte swapping, bypass mode, and microprocessor-like control interface.

Application-specific FIFOs, in addition to TI's Widebus™ FIFO products, offer space-saving surface-mount packaging and multiple-speed sorts for ease of design.

For FIFO data sheets, see the 1996 *High-Performance FIFO Memories Data Book*, literature number SCAD003C.

FIFO

ows Horn	NO.	DEVIC			A	VAILABIL	.ITY			LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	PLCC	QFP	TQFP	REFERENCE
SN74ABT3611	132, 120	64 × 36 Clocked FIFO						V	~	SCBS127D
SN74ABT3612	132, 120	64 × 36 × 2 Clocked Bidirectional FIFO						V	V	SCBS129F
SN74ABT3613	132, 120	64 × 36 Clocked FIFO						V	~	SCBS128E
SN74ABT3614	132, 120	64 × 36 × 2 Clocked Bidirectional FIFO	V	les suess a	t exten			V	V	SCBS126F
SN74ABT7819	80, 80	512 × 18 × 2 Clocked Bidirectional FIFO		9.31	T THE			V	V	SCBS125D
SN74ACT3622	132, 120	256 × 36 × 2 Clocked Bidirectional FIFO	e II.	\$ 50 st	159			V	V	SCAS247C
SN74ACT3631	132, 120	512 × 36 Clocked FIFO	ME SHE	SD 473 B	E 10	13.11		V	V	SCAS246F
SN74ACT3632	132, 120	512 × 36 × 2 Clocked Bidirectional FIFO	V		3 12			V	V	SCAS224C
SN74ACT3638	132, 120	512 × 32 × 2 Clocked Bidirectional FIFO		PERMIT	(5) (5) (5) (6) (6) (6) (6) (6) (6) (6) (6) (6) (6			V	V	SCAS228C
SN74ACT3641	132, 120	1K × 36 Clocked FIFO	V	O'CHE	UK			V	V	SCAS338B
SN74ACT7801	68	1K × 18 Clocked FIFO	19 18011	JUJS III	UITIU		V			SCAS111
SN74ACT7803	56	512 × 18 Clocked FIFO	JIU-U	G Q1 2	(Unit	~				SCAS191A
SN74ACT7805	56	256 × 18 Clocked FIFO	MOI	HI UE	GHO	V	ETIL	Hai		SCAS201
SN74ACT7807	44, 64	2K × 9 Clocked FIFO	a I down 1	lan in the	auties.		V		V	SCAS200B
SN74ACT7811	68, 80	1K × 18 Clocked FIFO	or the second	nd day	47.1		V		V	SCAS151C
SN74ACT7813	56	64 × 18 Clocked FIFO	DUNIO	THERE	10/107	V				SCAS199
SN74ACT7881	68, 80	1K × 18 Clocked FIFO	V	generally.	17500		V		V	SCAS227C
SN74ACT7882	68, 80	2K × 18 Clocked FIFO	STIM AS	W3 4770	AU1 + 17		V		V	SCAS445A
SN74ALVC7803	56	3.3-V 512 × 18 Clocked FIFO	Upca	Duide	KONETT	~		MINE		SDAS274A
SN74ALVC7805	56	3.3-V 256 × 18 Clocked FIFO		or Division M		V				SCAS436B
SN74ALVC7813	56	3.3-V 64 × 18 Clocked FIFO	rup ii	CULTUR	dala	V				SCAS436B
SN74ACT2226	24	64 × 1 Clocked FIFO	e Billi	PDC QU	V					SCAS219B
SN74ACT2227	28	64 × 1 Clocked FIFO		militae	V			1.16		SCAS220B
SN74ACT2228	24	256 × 1 Clocked FIFO	ciels	nais	V				Bir I	SCAS219B
SN74ACT2229	28	256 × 1 Clocked FIFO	eto a silvera	mell sh	V					SCAS220B
SN74ABT7820	80, 80	512 × 18 × 2 Strobed Bidirectional FIFO		-	- 1204		V		V	SCAS445A
SN74ACT2235	44, 64	1K × 9 × 2 Strobed Bidirectional FIFO					V		V	SCAS148C
SN74ACT2236	44	1K × 9 × 2 Strobed FIFO					V		10.9	SCAS149A
SN74ACT7802	68, 80	1K × 18 Strobed FIFO					V		V	SCAS187B
SN74ACT7804	56	512 × 18 Strobed FIFO				V				SCAS204A
SN74ACT7806	56	256 × 18 Strobed FIFO				V				SCAS438A
SN74ACT7808	44, 64	2K × 9 Strobed FIFO					V		V	SCAS205B
SN74ACT7814	56	64 × 18 Strobed FIFO				V		41.00		SCAS209A

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH = 52 pins
PAG = 64 pins
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins
PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



FIFO

DEMOS	NO.	FUNCTION			A	AILABIL	LITY			LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	PLCC	QFP	TQFP	REFERENCE
SN74ALVC7804	56	3.3-V 512 × 18 Strobed FIFO				V				SCAS432
SN74ALVC7806	56	3.3-V 256 × 18 Strobed FIFO				V	11:116			SCAS437C
SN74ALVC7814	56	3.3-V 64 × 18 Strobed FIFO				V				SCAS462
SN74ALS2238	40, 44	32 × 9 × 2 Bidirectional Strobed FIFO, 40 MHz		~			~			SCAS250D
SN74LS224A	16	16 × 4 Synchronous Strobed FIFO, 10 MHz	~	~						SDLS023
SN74ACT72211L	32	512 × 9 Synchronous FIFO					V			SCAS222
SN74ACT72221L	32	1K × 9 Synchronous FIFO					V			SCAS222
SN74ACT72231L	32	2K × 9 Synchronous FIFO					~			SCAS222
SN74ACT72241L	32	4K × 9 Synchronous FIFO					V			SCAS222
SN74ACT7200L	28, 28, 32	256 × 9 Asynchronous FIFO		~	~		~	MIL		SCAS221A
SN74ACT7201LA	28, 28, 32	512 × 9 Asynchronous FIFO		~	~		V			SCAS221A
SN74ACT7202LA	28, 28, 32	1K × 9 Asynchronous FIFO		V	V		V			SCAS221A
SN74ACT7203L	28, 32	2K × 9 Asynchronous FIFO		~			V			SCAS226A
SN74ACT7204L	28, 32	4K × 9 Asynchronous FIFO		V			V			SCAS226A
SN74ACT7205L	28, 32	8K × 9 Asynchronous FIFO		V			V			SCAS221A
SN74ACT7206L	28, 32	16K × 9 Asynchronous FIFO		V			V			SCAS226A
SN74ALS232B	16, 16, 20	16 × 4 Asynchronous FIFO, 40 MHz		V	V		V			SCAS251
SN74ALS233B	16, 16, 20	16 × 5 Asynchronous FIFO, 40 MHz		V	V		V			SCAS253
SN74ALS236	16	64 × 4 Asynchronous FIFO, 30 MHz		~	V		V			SDAS107A
SN74ALS2232A	24, 28	64 × 8 Asynchronous FIFO, 40 MHz		~			V			SCAS248
SN74ALS2233A	28, 28	64 × 9 Asynchronous FIFO, 40 MHz		V			V			SCAS249
SN74S225	20	16 × 5 Asynchronous FIFO, 10 MHz		V						SDLS207

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package) DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins = 64 pins PAH PAG PM PN

PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



PIPO

			3.3-V 256 x 18 Stroked FIFO	

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CEPP criente quad fut padeuge)
PR = 50 pins
PR = 50 pins
PQ = 100/132 pins
BCNC (crient-cuttice integrated ofn
D = N/14/16 pins
D = N/14/16 pins

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fuotienal soliticuloss) 100 arigē - y80

PAG = 64 pins
PA = 54 pins
PB = 60 pins
PCA PZ = 100 pixs

Mil. – refer to page 4-1 for minery package descriptor and university



GTL Gunning-Transceiver-Logic Technology

GTL technology is a new reduced-voltage switching standard that provides high-speed, point-to-point communications with low power dissipation. TI offers GTL/TTL translators to interface with the TTL-based subsystems. This enables designers to use the GTL-switching standards for speed-sensitive subsystems and to use the translators to interface with the rest of the system.

GTL devices have innovative circuitry, such as bus hold on the inputs to eliminate the need for external pullup resistors for floating inputs, which reduces power, cost, and board-layout time. Output edge-rate control (OECTM) is offered on the outputs to reduce electromagnetic interference (EMI) caused by the high frequencies of GTL.

Industry-leading packaging such as the shrink small-outline package (SSOP) and thin shrink small-outline package (TSSOP) is available for higher performance and reduced board space.

For GTL data sheets, see the 1997 GTL, BTL, and ETL Logic Data Book, literature number SCED004.

SSTL Series-Stub Terminated Logic

GTL/SSTL

DEVICE	NO.	FUNCTION		LITERATURE		
DEVICE	PINS	FUNCTION	MIL	SSOP	TSSOP	REFERENCE
SN74GTL16612	56	18-Bit Universal Bus Transceiver With OEC™	+	V	V	SCBS480E
SN74GTL16616	56	17-Bit Universal Bus Transceiver With Buffered Clock Outputs and OEC™	+	V	V	SCBS481D
SN74GTL16622	64	18-Bit LVTTL-to-GTL/GTL+ Registered Transceiver With OEC™		+	+	SCES049C
SN74GTL16922	64	18-Bit LVTTL-to-GTL/GTL+ Registered Transceiver With 5-V Tolerance and OEC™		+	+	SCBS673A
SN74GTL16923	64	18-Bit LVTTL-to-GTL/GTL+ Registered Transceiver With 5-V Tolerance and OEC™		+	+	SCBS674A
		Yechnology				
SN74SSTL16837	64	20-Bit SSTL_3 Universal Bus Driver			+	SCBS675

offers GTL/TTL translators to interface with the TTL-based subsystems. This shables designers to use the GTL-ewitching standards for speed-sensitive subsystems and to use the translators to interface with the rest of the system.

3TL devices have innovative circuitry, such as bus hold on the inputs to

eliminate the need for external pullup resistors for floating inputs, which reduces power, cost, and board-layout time. Output edge-rate control (OECra) is offered on the outputs to reduce electromagnetic interference (EMI) caused

Industry-leading packaging such as the shrink small-outline package (SSOP) and thin shrink small-outline package (TSSOP) is available for higher performance and reduced board space.

For GTL data sheets, see the 1997 GTL, BTL, and ETL Logic Data Book, literature number SCED004.

commercial package description and availability

PDIP (plastic dual-in-line package) QFP (plastic quad flat package) SOT (small-outline transistor) TSSOP (thin shrink small-outline package) N = 14/16/20 pins NT = 24/28 pins RC = 52 pins DBV = 5 pins PW = 8/14/16/20/24/28 pins PH = 80 pins DGG = 48/56/64 pinsTQFP (plastic thin quad flat package) NP = 28 pins PQ = 100/132 pinsTVSOP (thin very small-outline package) PAH = 52 pins PLCC (plastic leaded chip carrier) SOIC (small-outline integrated circuit) DGV = 14/16/20/24/48/56 pins PAG = 64 pins FN = 20/28/44/52/68/84 pins D = 8/14/16 pins DW = 16/20/24/28 pinsDBB = 80/100 pinsPM = 64 pins PN = 80 pins schedule PCA, PZ = 100 pins SSOP (shrink small-outline package) = 120 pins = Now DB = 14/16/20/24/28/30/38 pins MIL - refer to page 4-1 for military + = Planned DL = 28/48/56 pins package description and availability



HC/HCT High-Speed CMOS Logic

For low-power logic requirements, TI offers a full family of HC/HCT logic. Over 100 device types are available, including gates, latches, flip-flops, buffer/drivers, counters, multiplexers, transceivers, and registered transceivers.

The HC family offers CMOS-compatible inputs and the HCT family offers TTL-compatible inputs.

For HC/HCT data sheets, see the 1996 AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book, literature number SCLD004.

HC

IGIUD NO	NO.	DEVICE SEL		-	VAILAB	LITY		LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	TSSOP	REFERENCE
SN74HC00	14	Quad 2-Input Positive-NAND Gate	~	~	~	V	V	SCLS181A
SN74HC02	14	Quad 2-Input Positive-NOR Gate	V	~	V	V	~	SCLS076A
SN74HC03	14	Quad 2-Input Positive-NAND Gate With Open-Drain Outputs	V	~	V			SCLS077A
SN74HC04	14	Hex Inverter	V	~	V	V	V	SCLS078A
SN74HCU04	14	Unbuffered Hex Inverter	V	~	V			SCLS079A
SN74HC05	14	Hex Inverter With Open-Drain Outputs	~	~	V	V	V	SCLS080A
SN74HC08	14	Quad 2-Input Positive-AND Gate	V	~	V	V	V	SCLS081A
SN74HC10	14	Triple 3-Input Positive-NAND Gate	O V	V	V			SCLS083A
SN74HC11	14	Triple 3-Input Positive-AND Gate	100	~	V			SCLS084A
SN74HC14	14	Hex Inverter With Schmitt-Trigger	V	~	V	V	V	SCLS085A
SN74HC20	14	Dual 4-Input Positive-NAND Gate	V	~	V			SCLS086B
SN74HC21	14	Dual 4-Input Positive-AND Gate	V	V	V			SCLS087A
SN74HC27	14	Triple 3-Input Positive-NOR Gate	V	V	V			SCLS088A
SN74HC32A	14	Quad 2-Input Positive-OR Gate	V	~	V	V	V	Call
SN74HC42	16	4-to-10 BCD to Decimal Decoder	~	V	V			SCLS091A
SN74HC74	14	Dual D-Type Flip-Flop	2	V	V	V	V	SCLS094A
SN74HC86	14	Quad 2-Input Exclusive-OR Gate	V	V	~	V		SCLS100A
SN74HC109	16	Dual J-K Positive-Edge-Triggered Flip-Flop	V	V	V			SCLS098
SN74HC112	16	Dual J-K Negative-Edge-Triggered Flip-Flop	V	~	V			SCLS099A
SN74HC125	14	Quad Bus Buffer Gate (OE)	V	V	V	V	V	SCLS104A
SN74HC126	14	Quad Bus Buffer Gate (OE)	V	V	V	~	V	SCLS103A
SN74HC132	14	Quad 2-Input Positive-NAND Gate With Schmitt-Trigger Inputs	V	V	V	V	V	SCLS034B
SN74HC138	16	3-to-8 Decoder/Demultiplexer	V	V	V		V	SCLS107B
SN74HC139	16	Dual 2-to-4 Line Decoder/Demultiplexer	V	V	V	V	V	SCLS108A
SN74HC148	16	8-to-3 Line Priority Encoder	V	V	V			SCLS109C
SN74HC151	16	8-to-1 Data Selector/Multiplexer	V	V	V	V		SCLS110B
SN74HC153	16	Dual 4-to-1 Data Selector/Multiplexer	V	V	V		V	SCLS112A
SN74HC157	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	V			SCLS113A
SN74HC161	16	4-Bit Synchronous Binary Counter	V	V	V			SCLS297
SN74HC163	16	4-Bit Synchronous Binary Counter	V	V	V			SCLS298
SN74HC164	14, 16	8-Bit Parallel-Out Serial Shift Register	V	V	V			SCLS115A

commercial package description and availability

PDIP (plastic dual-in-line package)

N = 14/16/20 pins NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now

+ = Planned

QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins

PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins PAH PAG

PM = 64 pins

PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package)

PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



	NO.				VAILABI	LITY		LITERATURE
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	TSSOP	REFERENCE
SN74HC165	16	8-Bit Parallel-Load Shift Register	V	V	V	115-8	81 V	SCLS116B
SN74HC165	16	8-Bit Parallel-Load Shift Register	~	V	V	118-8	814	SCLS116B
SN74HC166	16	8-Bit Parallel-Load Shift Register	V	V	V	Octa	08	SCLS117A
SN74HC174	16	Hex D-Type Flip-Flop	~	V	1	ntoO	20	SCLS119A
SN74HC175	16	Quad D-Type Flip-Flop With Clear	~	~	V	Octa	00 V	SCLS299
SN74HC191	16	4-Bit Synchronous Up/Down Binary Counter	V	V	V	sp0-	24	SCLS121A
SN74HC193	16	4-Bit Synchronous Up/Down Binary Counter	V	V	V	Octo	24	SCLS122A
SN74HC240	20	Octal Buffer/Driver	V	V	V	V	20	SCLS128A
SN74HC241	20	Octal Buffer/ Driver	V	~	V	V	V20	SCLS300
SN74HC244A	20	Octal Buffer/Driver	V	~	V	V	081	Call
SN74HC245	20	Octal Bus Transceiver	OW.	V	V	V	814	SCLS131A
SN74HC251	16	8-to-1 Data Selector/Multiplexer	V	V	V	12-8	18	SCLS132A
SN74HC253	16	Dual 4-to-1 Data Selector/Multiplexer	V	V	V	14-8	16	SCLS133A
SN74HC257	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	V	V	11	SCLS349
SN74HC259	16	8-Bit Addressable Latch	OV	V .	V	V	NV	SCLS134A
SN74HC266	14	Quad 2-Input Exclusive-NOR Gate With Open-Drain Outputs	D ROM	V	V	gua.	16	SCLS135B
SN74HC273	20	Octal D-Type Flip-Flop With Clear	000	V	~	V	NV.	SCLS136A
SN74HC365	16	Hex Buffer/Driver	V	~	V			SCLS308A
SN74HC367	16	Hex Buffer/Driver	V	V	V			SCLS309A
SN74HC368	16	Hex Buffer/Driver	V	V	V			SCLS310
SN74HC373	20	Octal D-Type Transparent Latch	V	~	V	V	V	SCLS140A
SN74HC374	20	Octal D-Type Flip-Flop	V	V	V	V	V	SCLS141A
SN74HC377	20	Octal D-Type Flip-Flop With Clock Enable	V	V	V			SCLS307
SN74HC393	14	Dual 4-Bit Binary Counter	~	V	V	V		SCLS143A
SN74HC534	20	Octal D-Type Flip-Flop	~	V	V			SCLS311
SN74HC540	20	Octal Buffer/Driver	V	V	V			SCLS007A
SN74HC541	20	Octal Buffer/Driver	V	V	V	V	V	SCLS305
SN74HC563	20	Octal D-Type Transparent Latch	~	V	V			SCLS145A
SN74HC573A	20	Octal D-Type Transparent Latch	V	V	V	V	V	SCLS147A
SN74HC574	20	Octal D-Type Flip-Flop	V	~	V			SCLS148A
SN74HC590A	16	8-Bit Binary Counter	V	V	V			SCLS039B

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned

QFP (plastic quad flat package) RC = 52 pins PH = 80 pins

PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins

SOT (small-outline transistor)

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins PAH PAG PM = 64 pms PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



HC

and the control of	NO.	YTHEAHAVA			A	VAILABI	LITY		LITERATURE
DEVICE	PINS	FUNCTION STATES		MIL	PDIP	SOIC	SSOP	TSSOP	REFERENCE
SN74HC594	16	8-Bit Shift Register	19180	nit Re	8 V	V	1	18	SCLS040A
SN74HC595	16	8-Bit Shift Register	yoteig	V	· V	V		81 .	SCLS041A
SN74HC623	20	Octal Bus Transceiver	netaig	oit Re	V	~	1181-8	16	SCLS149A
SN74HC640	20	Octal Bus Transceiver		~	V	V	xeH	18	SCLS303
SN74HC645	20	Octal Bus Transceiver	(Class	V	~	V	Quar	81	SCLS304
SN74HC646	24	Octal Registered Bus Transceiver	n Binary Counter	woQ\c	~	V	113-1	16	SCLS150A
SN74HC652	24	Octal Registered Bus Transceiver	n Binary Counter	we(I) o	V	V	104	87	SCLS151A
SN74HC682	20	8-Bit Magnitude Comparator			V	V	stoO	20	SCLS018B
SN74HC684	20	8-Bit Magnitude Comparator			1	V	Octs	20	SCLS340
SN74HC688	20	8-Bit Magnitude Comparator		~	V.	V	~	· V	SCLS010A
SN74HC4020	16	14-Bit Asynchronous Binary Counter		~	~	V	aloC.	00	SCLS158A
SN74HC4040	16	12-Bit Asynchronous Binary Counter	1510	~	V	V	V	V	SCLS160A
SN74HC4060	16	14-Bit Asynchronous Binary Counter/Oscillator	lutiplexer	Ancier	V	~	Dual	81	SCLS161A
SN74HC4066	14	Quad Bilateral Analog Switch	Multiplemen	halosi	V	V	V	81V	SCLS325A
SN74HC7001	14	Quad 2-Input Positive-AND Gate		rigi	~	~	68-e	81	SCLS035A
SN74HC7002	14	Quad 2-Input Positive-NOR Gate	R Gate With Open	OV-ev	V	~	neus)	M	SCLS033B
SN74HC7032	14	Quad 2-Input Positive-OR Gate	Clear	tillA q	~	V	Octa	08	SCLS036A
SCLSSORA		N N 10		1	ravhi	2 halful	xels	16	SHIMHCISES

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins

N = 14/16/20 pin NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now
+ = Planned

QFP (plastic quad flat package) RC = 52 pins

PH = 80 pins PQ = 100/132 pins

DL = 28/48/56 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH = 52 pins PAG = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins

DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins



HCT

DEVICE	NO.	FUNCTION		AVAILABILITY LITERATU							
	PINS		MIL	PDIP	SOIC	SSOP	TSSOP	REFERENC			
SN74HCT00	14	Quad 2-Input Positive-NAND Gate		V	V	V	V	SCLS062A			
SN74HCT02	14	Quad 2-Input Positive-NOR Gate		V	V	V		SCLS065A			
SN74HCT04	14	Hex Inverter	~	~	V	V	V	SCLS042A			
SN74HCT08	14	Quad 2-Input Positive-AND Gate		V	V	V	V	SCLS063A			
SN74HCT14	14	Hex Inverter With Schmitt-Trigger	V	V	V	V	V	SCLS225A			
SN74HCT32	14	Quad 2-Input Positive-OR Gate	ı	~	V	V	V	SCLS064A			
SN74HCT74	14	Dual D-Type Flip-Flop		V	V	~	~	SCLS169A			
SN74HCT125	14	Quad Bus Buffer Gate (OE)		V	V			SCLS069B			
SN74HCT138	16	3-to-8 Decoder/Demultiplexer	V	~	V	~	~	SCLS171B			
SN74HCT139	16	Dual 2-to-4 Decoder/Demultiplexer		V	V	V	~	SCLS066A			
SN74HCT157	16	Quad 2-to-1 Data Selector/Multiplexer		V	V			SCLS071A			
SN74HCT240	20	Octal Buffer/ Driver	V	V	V			SCLS174A			
SN74HCT244	20	Octal Buffer/ Driver	~	V	V	V	~	SCLS175A			
SN74HCT245	20	Octal Bus Transceiver	V	V	V	V	V	SCLS020B			
SN74HCT257	16	Quad 2-to-1 Data Selector/Multiplexer		V	V			SCLS072A			
SN74HCT273	20	Octal D-Type Flip-Flop With Clear		V	V	V	~	SCLS068B			
SN74HCT373	20	Octal D-Type Transparent Latch	V	V	V	V		SCLS009A			
SN74HCT374	20	Octal D-Type Flip-Flop	V	V	V	~		SCLS005A			
SN74HCT377	20	Octal D-Type Flip-Flop With Clock Enable		V	V			SCLS067B			
SN74HCT540	20	Octal Buffer/ Driver	~	V	V			SCLS008A			
SN74HCT541	20	Octal Buffer/ Driver	V	~	V	V		SCLS306			
SN74HCT573	20	Octal D-Type Transparent Latch		V	V	V	V	SCLS176A			
SN74HCT574	20	Octal D-Type Flip-Flop		V	V	BEE	V	SCLS177B			
SN74HCT623	20	Octal Bus Transceiver		~	V			SCLS016A			
SN74HCT645	20	Octal Bus Transceiver		V	V			SCLS019A			
SN74HCT646	24	Octal Registered Bus Transceiver		~	V			SCLS178A			
SN74HCT652	24	Octal Registered Bus Transceiver		V	V			SCLS179A			

commercial package description and availability

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schedule

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DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH = 52 pins
PAG = 64 pins
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins
PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins



			Dust 2-to-4 Decodes/Demultiplaxor	
		V		



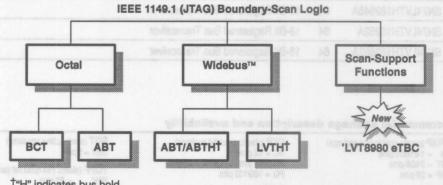
IEEE 1149.1 (JTAG) Boundary-Scan Logic Devices

The IEEE 1149.1 (JTAG) boundary-scan logic family of octal, Widebus™, and scan-support functions incorporates circuitry that allows these devices and the electronic systems in which they are used to be tested without reliance on traditional probing techniques.

Bus-interface logic devices are available in BCT, ABT, and LVT technologies, in 8-, 18-, and 20-bit options of the standard buffers, latches, and transceivers, Package options for these devices include plastic dual in-line (PDIP), small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin quad flatpack (TQFP). The scan-support functions include devices for controlling the test bus, performing at-speed functional testing, and partitioning the scan path into smaller, more manageable segments.

Over 30 devices, composed of a wide selection of BCT and ABT octals, ABT and LVT Widebus™, and each of the scan-support functions, are available. Bus-hold and series-damping resistor features also are available.

For JTAG data sheets, see the 1997 Boundary-Scan Logic IEEE Std 1149.1 (JTAG), literature number SCTD002A.



†"H" indicates bus hold

IEEE 1149.1 (JTAG)

GRUD MOITS	NO.	S HOIVE					LITERATURE			
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	SSOP	TSSOP	PLCC	TQFP	REFERENCE
Widebus™ Devices										
SN74ABT18245A	56	18-Bit Bus Transceiver	~			~	~			SCBS110F
SN74ABT18640	56	18-Bit Inverting Bus Transceiver				~	~			SCBS267C
SN74ABTH18502A	64	18-Bit Universal Bus Transceiver	V						~	SCBS164D
SN74ABTH18504A	64	20-Bit Universal Bus Transceiver	25 26		GAN III				V	SCBS165C
SN74ABTH18646A	64	18-Bit Registered Bus Transceiver	V	MU	ou				V	SCBS166D
SN74ABTH18652A	64	18-Bit Registered Bus Transceiver							V	SCBS167D
SN74ABTH182502A	64	18-Bit Universal Bus Transceiver	TL) 1.041	1 333	leniT			Mark	V	SCBS164D
SN74ABTH182504A	64	20-Bit Universal Bus Transceiver	offenult in	oddns	scan-				V	SCBS165C
SN74ABTH182646A	64	18-Bit Registered Bus Transceiver	neteya di	ectron	le orb				V	SCBS166D
SN74ABTH182652A	64	18-Bit Registered Bus Transceiver	robing te	g land	libert				V	SCBS167D
SN74LVTH18245	56	18-Bit Bus Transceiver	h alaat m	sobole.	Lacid .	+	+			SCBS161C
SN74LVTH182245	56	18-Bit Bus Transceiver	utt-Locks	no -61	D rd	+	+			SCBS161C
SN74LVTH18502A	64	18-Bit Universal Bus Transceiver	antin	n one	Dank				V	SCBS668
SN74LVTH182502A	64	18-Bit Universal Bus Transceiver	ovosini a	rillion-	Herris		- 2		V	SCBS668
SN74LVTH18504A	64	20-Bit Universal Bus Transceiver	tun-linma	derively	e nicti				V	SCBS667
SN74LVTH182504A	64	20-Bit Universal Bus Transceiver	i nonou	e-mean	oriT				V	SCBS667
SN74LVTH18512	64	18-Bit Universal Bus Transceiver	31-2000	pairm	ohen		+			SCBS671
SN74LVTH182512	64	18-Bit Universal Bus Transceiver	enem en	er, mo	llsme		+			SCBS671
SN74LVTH18514	64	20-Bit Universal Bus Transceiver					+			SCBS670
SN74LVTH182514	64	20-Bit Universal Bus Transceiver	vices, con	30 de	Over		+			SCBS670
SN74LVTH18516	64	18-Bit Universal Bus Transceiver	idebus ^m ,	W TV.	and t		+			SCBS672
SN74LVTH182516	64	18-Bit Universal Bus Transceiver	sehes br	is blor	Heu@		+			SCBS672
SN74LVTH18640	56	18-Bit Inverting Bus Transceiver			land.	+	+			SCBS310B
SN74LVTH182640	56	18-Bit Inverting Bus Transceiver	व्याव होहि	DEMI	0.10%	+	+			SCBS310B
SN74LVTH18646A	64	18-Bit Registered Bus Transceiver	All Almia	em Ve	mit uj				+	SCBS311B
SN74LVTH182646A	64	18-Bit Registered Bus Transceiver							+	SCBS311B
SN74LVTH18652A	64	18-Bit Registered Bus Transceiver							+	SCBS312B
SN74LVTH182652A	64	18-Bit Registered Bus Transceiver	1	u calendario	1		ST POR		+	SCBS312B
			7 1.4							

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

= Now + = Planned QFP (plastic quad flat package) RC = 52 pins

PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package) PAH

= 52 pins = 64 pins PAG = 64 pins = 80 pins PM PN PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins



IEEE 1149.1 (JTAG)

DEMOS	NO.	FUNCTION		LITERATURE						
DEVICE	PINS		MIL	PDIP	SOIC	SSOP	TSSOP	PLCC	TQFP	REFERENCE
Octal Bus-Interface	Devices									
SN74BCT8240A	24	Octal Buffer/Driver	V	V	~					SCBS067D
SN74BCT8244A	24	Octal Buffer/Driver	V	~	V					SCBS042E
SN74BCT8245A	24	Octal Bus Transceiver	~	~	V					SCBS043E
SN74BCT8373A	24	Octal D-Type Latch	V	~	V					SCBS044F
SN74BCT8374A	24	Octal D-Type Flip-Flop	V	V	V					SCBS045E
SN74ABT8245	24	Octal Bus Transceiver	~		V					SCBS124C
SN74ABT8543	28	Octal Registered Bus Transceiver	V	-	~	V				SCBS120E
SN74ABT8646	28	Octal Registered Bus Transceiver	V		V	V				SCBS123E
SN74ABT8652	28	Octal Registered Bus Transceiver	~		V	~				SCBS122E
SN74ABT8952	28	Octal Registered Bus Transceiver			~	V				SCBS121D
Scan-Support Devi	ces									
SN74LVT8980	24	JTAG Embedded Test Bus Controller	V		~					SCBS676
SN74ACT8990	44	JTAG Test Bus Controller	~					~	li li li	SCAS190C
SN74ACT8994	28	Digital Bus Monitor						~		SCAS196D
SN74ABT8996	24	Addressable Scan Port	~		V		~			SCBS489A
SN74ACT8997	28	Scan-Path Linker	~	~	V					SCAS157C
SN74ACT8999	28	Scan-Path Selector With 8-Bit Bidirectional Data Buses	~	~	~					SCAS158C

commercial package description and availability

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TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



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(DATL) 1449.1 (JTAG)

			V		

PGSP (please duel-In-line podrage)
14 = 14/2500 pins
14 = 24/2500 pins
147 = 24/25 pins
147 = 23 pins
144 = 24/26/44 pins
144 = 24/26/44 pins
145 = 14/26/44 pins
145

PS = 400 por PD = 100132 pins BOTC (since cuttous inagensed choos D = 81412 pins CML - Exercises sins

60P (elock evelt outro podros) 8 × várdozakyadolakale

TBSOP (TEN SIMPLE PW -- STAYTS(2005) TUSCO -- ASSESSA (SI

TVROP (Ith very email-outle DGV = 14/1620/244688 per DBB = 80/100 pins

MIL - polar to page 4-1 for military passage describins and availabilities

INSTRUMENTS

LS Low-Power Schottky Logic

While the overall demand for LS products is declining, there remains significant interest in the marketplace for many of the LS functions. TI will continue to supply LS products as long as there is an appropriate level of market demand for them.

The LS family is not recommended for new designs.

14

For LS data sheets, contact the Product Information Center at (972) 644-5580.

LS

DEVICE	NO. PINS	FUNCTION	MIL	AVAIL	ABILITY	SSOP	LITERATURE
SN74LS00	14	Quad 2-Input Positive-NAND Gate	V	V	V	V	SDLS025
SN74LS01	14	Quad 2-Input Positive-NAND Gate With Open-Collector Outputs	V	V	V		SDLS026
SN74LS02	14	Quad 2-Input Positive-NOR Gate	V	V	V		SDLS027
SN74LS03	14	Quad 2-Input Positive-NAND Gate With Open-Collector Outputs	V	V	V	Berri	SDLS028
SN74LS04	14	Hex Inverter	V	V	V		SDLS029
SN74LS05	14	Hex Inverter With Open-Collector Outputs	V	V	V		SDLS030
SN74LS06	14	Hex Inverter With Open-Collector Outputs	V	V	V	V	SDLS020A
SN74LS07	14	Hex Buffer With Open-Collector Outputs	V	V	V	V	SDLS021A
SN74LS08	14	Quad 2-Input Positive-AND Gate	V	V	V		SDLS033
SN74LS09	14	Quad 2-Input Positive-AND Gate With Open-Collector Outputs	~	V	V		SDLS034
SN74LS10	14	Triple 3-Input Positive-NAND Gate	V	V	V		SDLS035
SN74LS11	14	Triple 3-Input Positive-AND Gate	~	V	V	Print.	SDLS131
SN74LS14	14	Hex Inverter With Schmitt Trigger	~	V	V	V	SDLS049
SN74LS19A	14	Hex Inverter With Schmitt Trigger		V	V		SDLS138
SN74LS20	14	Dual 4-Input Positive-NAND Gate	V	V	V		SDLS079
SN74LS21	14	Dual 4-Input Positive-AND Gate	V	V	V		SDLS022
SN74LS26	14	Quad 2-Input NAND Gate	~	V	V		SDLS087
SN74LS27	14	Triple 3-Input Positive-NOR Gate	V	~	V		SDLS089
SN74LS30	14	8-Input Positive-NAND Gate	V	V	~		SDLS099
SN74LS31	14	Delay Element		~	V		SDLS157
SN74LS32	14	Quad 2-Input Positive-OR Gate	V	V	V		SDLS100
SN74LS33	14	Quad 2-Input NOR Gate With Open-Collector Outputs	V	V	V		SDLS101
SN74LS37	14	Quad 2-Input Positive-NAND Gate	V	V	V		SDLS103
SN74LS38	14	Quad 2-Input Positive-NAND Gate With Open-Collector Outputs	V	V	~		SDLS105
SN74LS42	16	4-to-10 BCD-to-Decimal Decoder	V	~	V		SDLS109
SN74LS47	16	BCD 7-Segment Decoder/Driver	V	V	~		SDLS111
SN74LS51	14	Dual 2-Input and Dual 3-Input AND/OR Gate	V	V	V		SDLS113
SN74LS73A	14	Dual J-K Flip-Flop	~	~	V		SDLS118
SN74LS74A	14	Dual D-Type Flip-Flop	~	V	V		SDLS119
SN74LS75	16	4-Bit D-Type Latch	V	~	V		SDLS120
SN74LS85	16	4-Bit Magnitude Comparator	V	V	V	ALC:	SDLS123

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
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NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

= Now + = Planned QFP (plastic quad flat package)
RC = 52 pins
PH = 80 pins
PQ = 100/132 pins

SOIC (small-outline integrated circuit) D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH = 52 pins
PAG = 64 pins
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins
PCB = 120 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



DEVICE	NO. PINS	STUBBALIAVA SESS SHESS JEES FUNCTION SECTIONS	MIL	AVAIL	ABILITY	SSOP	LITERATURE REFERENCE
SN74LS86A	14	Quad 2-Input Exclusive-OR Gate	V	V	V	16	SDLS124
SN74LS90	14	Decade Counter	V	V	V	16	Call
SN74LS92	14	Divide-By-12 Counter	Gover	V	V	81	Call
SN74LS93	14	4-Bit Binary Counter	V	onev m	V	16	Call
SN74LS107A	14	Dual J-K Flip-Flop	V	V	V	83	SDLS036
SN74LS109A	16	Dual J-K Flip-Flop	V	V	V	16	SDLS037
SN74LS112A	16	Dual J-K Negative-Edge-Triggered Flip-Flop	V	V	V	16	SDLS011
SN74LS122	14	One-Shot Multivibrator	V	V	V	20	SDLS043
SN74LS123	16	Dual Monostable Multivibrator	V	V	V	20	SDLS043
SN74LS125A	14	Quad Bus Buffer Gate (OE)	V	V	V	44	SDLS044
SN74LS126A	14	Quad Bus Buffer Gate (OE)	V	V	V	00	SDLS044
SN74LS132	14	Quad 2-Input Positive-NAND With Schmitt Trigger	V	V	V	DS -	SDLS047
SN74LS136	14	Quad Exclusive-OR Gate With Open-Collector Outputs	V	V	V	81	SDLS048
SN74LS137	16	3-to-8 Decoder/Demultiplexer With Address Latch	V	V	V	25	SDLS132
SN74LS138	16	3-to-8 Decoder/Demultiplexer	V	V	V	91	SDLS014
SN74LS139A	16	Dual 2-to-4 Decoder/Demultiplexer	iosi v s	0 V 0	V	16	SDLS013
SN74LS145	16	BCD-to-Decimal Decoder/Driver	100 V S	~	~	10	SDLS051
SN74LS148	16	8-to-3-Line Priority Encoder	V .	~	IV	16	Call
SN74LS151	16	8-to-1 Data Selector/Multiplexer		31	V	147	SDLS054
SN74LS153	16	Dual 4-to-1 Data Selector/Multiplexer	OV.	V	IEVO	20	SDLS055
SN74LS155A	16	Dual 1-to-4 Decoder	V	V	V	81	SDLS057
SN74LS156	16	Dual 2-to-4-Line Decoder/Demultiplexer With Open-Collector Outputs	0	V	V	14	SDLS057
SN74LS157	16	Quad 1-of-2 Data Selector/Multiplexer	100	V	V	16	SDLS058
SN74LS158	16	Quad 1-of-2 Data Selector/Multiplexer	0 Van	V	V	97	SDLS058
SN74LS161A	16	4-Bit Synchronous Binary Counter	00 1	V	V	81	SDLS060
SN74LS163A	16	4-Bit Synchronous Binary Counter	V	V	V	18	SDLS060
SN74LS164	14	8-Bit Parallel-Out Serial Shift Register	V	V	V	16	SDLS061
SN74LS165A	16	8-Bit Parallel-Load Shift Register	V	~	V	20	Call
SN74LS166A	16	8-Bit Parallel-Load Shift Register	V	V	V	10	SDLS063
SN74LS169B	16	4-Bit Synchronous Up/Down Binary Counter	V	le V vin	V	20	SDLS134
SN74LS173A	16	4-Bit D-Type Latch	V	V	V	10	SDLS067

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DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH PAG = 52 pins = 64 pins

PM = 64 pins

PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



LS

DEVICE	NO. PINS	PILESA BAVA OLOS PIOS BAVA FUNCTION		MIL	AVAIL	ABILITY	SSOP	LITERATURE REFERENCE
SN74LS174	16	Hex D-Type Flip-Flop	-OR Gets	V	V	V	14	SDLS068
SN74LS175	16	Quad D-Type Flip-Flop		V		V	14	SDLS068
SN74LS191	16	4-Bit Synchronous Up/Down Binary Counter		V	018	V	14	SDLS072
SN74LS193	16	4-Bit Synchronous Up/Down Binary Counter		V	100 V 811	V	14	SDLS074
SN74LS194A	16	4-Bit Bidirectional Universal Shift Register		1	V	L W	14	SDLS075
SN74LS195A	16	4-Bit Bidirectional Universal Shift Register		V	V	V	81	SDLS076
SN74LS221	16	Dual Monostable Multivibrator	- Inggerad Filp-Flop	V	V	V	81	SDLS213
SN74LS240	20	Octal Buffer/Driver		V	V	V	M	SDLS144
SN74LS241	20	Octal Buffer/Driver	totator	V	V	V	16	SDLS144
SN74LS243	14	Quad Bus Transceiver	(B)	V	NV V	V	Tri .	SDLS145
SN74LS244	20	Octal Buffer/Driver	(30	·V	V	V	14	SDLS144
SN74LS245	20	Octal Bus Transceiver	AND With Schmitt Trigg	V	V	V	V	SDLS146A
SN74LS247	16	BCD-to-7-Segment Decoder	is With Open-Collector C	V	V	V	H	SDLS083
SN74LS251	16	1-of-8 Data Selector/Multiplexer	plexer With Address Late	V	V	V	81	SDLS085
SN74LS253	16	Dual 4-to-1 Data Selector/Multiplexer	olexer	V	V	3 V3	16	SDLS147
SN74LS257B	16	Quad 2-to-1 Data Selector/Multiplexer	neutiplexer	V	· V	V	16	SDLS148
SN74LS258B	16	Quad 2-to-1 Data Selector/Multiplexer	nevh@her	ov.	- V	V	16	SDLS148
SN74LS259B	16	8-Bit Addressable Latch	rebo	V	V	V	81	SDLS086
SN74LS266	14	Quad 2-Input Exclusive-NOR Gate	texeloffi	V	V	-V	61	SDLS151
SN74LS273	20	Octal D-Type Flip-Flop	or/Multiplexer	V	V	V	16	SDLS090
SN74LS279A	16	Quad Set/Reset Latch		V	V	V	16	SDLS093
SN74LS280	14	9-Bit Parity Generator/Checker	of Demuliplener With Oy	ov.	30 V	V	81	SDLS152
SN74LS283	16	4-Bit Binary Full Adder	15xalqifiuMnot	V	V	V	16	SDLS095
SN74LS292	16	31-Bit Programmable Counter	JoriMudipleser	a Selec	V	bauO	16	SDLS153
SN74LS294	16	16-Bit Programmable Counter	ry Counter	us Bine	V	4.31.5	01	SDLS153
SN74LS297	16	Digital Phase-Lock Loop	ry Countier	us Bino	V	6 1/E-y	ar	SDLS155
SN74LS298	16	Quad 2-Input Multiplexer With Storage	Shill Register	V	01	V	14	SDLS098
SN74LS299	20	8-Bit Universal Shift/Storage Register	refelge#	V	V	V	18	SDLS156
SN74LS321	16	Crystal-Controlled Oscillator	Register	MIE be	V	9 88 P	10	Call
SN74LS323	20	8-Bit Universal Shift/Storage Register	Josep Blooky Counter	V	V	V	18	SDLS160
SN74LS348	16	8-to-3-Line Encoder		V	V	V	61	SDLS161

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
NT = 24/28 pins

NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package) RC = 52 pins PH = 80 pins PQ = 100/132 pins

SOIC (small-outline integrated circuit)

D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH PAG = 52 pins = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



A 1740	NO.	YTLEGARAVA		AVAILABILITY OF			LITERATURE	
DEVICE	PINS	SIGN SIGN LINE		MIL	PDIP	SOIC	SSOP	REFERENCE
SN74LS365A	16	Hex Buffer/Driver	rotallio	V	V-	V	14	SDLS102
SN74LS367A	16	Hex Buffer/Driver	rotello	V	V	V	16	SDLS102
SN74LS368A	16	Hex Buffer/Driver		V	V	-	20	SDLS102
SN74LS373	20	Octal D-Type Transparent Latch		V	V	V	20	SDLS165
SN74LS374	20	Octal D-Type Flip-Flop	Wilk Op	V	V	V	20	SDLS165
SN74LS375	16	4-Bit Bistable Latch	With Ope	V	V	0	20	SDLS166
SN74LS377	20	Octal D-Type Flip-Flop With Clock Enable	With Ope	V	V	V	20	SDLS167
SN74LS378	16	Hex D-Type Flip-Flop With Clock Enable	With Op	V	V	V	os .	SDLS167
SN74LS379	16	Quad D-Type Flip-Flop With Clock Enable		V	V	W	20	SDLS167
SN74LS382	20	4-Bit Arithmetic Logic Unit	viscenstī	ed Bus	V	listoQ	24	Call
SN74LS390	16	Dual 4-Bit Decade Counter	Transcelv	V	V	V	24	SDLS107
SN74LS393	14	Dual 4-Bit Binary Counter	เสรออกเราโ	V	V	V	24	SDLS107
SN74LS396	16	Octal Storage Register	viecenay?	V	V	Gotal	24	SDLS173
SN74LS399	16	Quad 2-Input Multiplexer	7	100	V	V	16	SDLS174
SN74LS423	16	Retriggerable Multivibrator		V	V	V	81	SDLS175
SN74LS442	20	Bus Transceiver		redak	V .	18 V	24	SDLS176
SN74LS465	20	Octal Buffer/Driver		tolsk	V 2	V	24	SDLS179
SN74LS466	20	Bus Transceiver	10/818	Comp	V	V	DS	SDLS179
SN74LS540	20	Octal Buffer/Driver	tolsto	V	V	V	OS .	SDLS180
SN74LS541	20	Octal Buffer/Driver	ју Остра	V	V	V	82	SDLS180
SN74LS590	16	8-Bit Binary Counter With 3-State Output Register	10	V	00	V	OS	SDLS003
SN74LS592	16	Binary Counter With Input Register	r Binary C	V	V	V	20	SDLS004
SN74LS593	20	8-Bit Binary Counter With 3-State I/O Register		V	V	V		SDLS004
SN74LS594	16	8-Bit Shift Register With Output Register			V	V		SDLS005
SN74LS595	16	8-Bit Shift Register With 3-State Output Register		V	V	V		SDLS006
SN74LS596	16	Octal Shift Register			V	Maj in		SDLS006
SN74LS597	16	Shift Register With Input Latch		~	V	V		SDLS007
SN74LS598	20	Shift Register With Input Latch		~	~	V		SDLS007
SN74LS599	16	Shift Register With Output Latch			~	V		SDLS005
SN74LS623	20	Octal Bus Transceiver			V	V		SDLS185
SN74LS624	14	Voltage-Controlled Oscillator		V	V	V		SDLS186

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D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor)
DBV = 5 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins

= 64 pins PM = 80 pins PN PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



LS

MUDARETLI	NO.	KARTYARIA			AVAILABILITY			LITERATURE
DEVICE	PINS	FUNCTION		MIL	PDIP	SOIC	SSOP	REFERENCI
SN74LS628	14	Voltage-Controlled Oscillator		V	V	70	81	SDLS186
SN74LS629	16	Voltage-Controlled Oscillator		~	V	V	31	SDLS186
SN74LS640	20	Octal Bus Transceiver		1	V	V	81	SDLS189
SN74LS640-1	20	Octal Bus Transceiver	riota.) the	eqener	W-C	0	20	SDLS189
SN74LS641	20	Octal Bus Transceiver With Open-Collector Outputs		V	V	V	20	SDLS189
SN74LS641-1	20	Octal Bus Transceiver With Open-Collector Outputs		data	V .	V	31	SDLS189
SN74LS642	20	Octal Bus Transceiver With Open-Collector Outputs	Willi Cłosk Eruble	V	W-O	V	09	SDLS189
SN74LS642-1	20	Octal Bus Transceiver With Open-Collector Outputs	Villa Glock Brable	rgo/Alop	V	V	16	SDLS189
SN74LS645	20	Octal Bus Transceiver	With Clock Enable	V	V	V	10	SDLS189
SN74LS646	24	Octal Registered Bus Transceiver	flrit.	Logic I	V	V	20	SDLS190
SN74LS647	24	Octal Registered Bus Transceiver	notine	ide Coi	V	V	ar	SDLS190
SN74LS648	24	Octal Registered Bus Transceiver	teh	ry Ceur	V	V	M	SDLS190
SN74LS652	24	Octal Registered Bus Transceiver		iedalei	V 2	V	81	SDLS191
SN74LS669	16	4-Bit Up/Down Counter	16	V	V	~	ar	SDLS192
SN74LS670	16	4-By-4 Register File	1013	V	V .	V	81	SDLS193
SN74LS673	24	16-Bit Shift Register		V	V	T.V	20	SDLS195
SN74LS674	24	16-Bit Shift Register		~	OV.	V	20	SDLS195
SN74LS682	20	8-Bit Magnitude Comparator		V	V	TeV.	08-	SDLS008
SN74LS684	20	8-Bit Magnitude Comparator		V	V	V	20	SDLS008
SN74LS686	24	Octal Magnitude/Identity Comparator		YEV	V	V	20	SDLS008
SN74LS688	20	8-Bit Identity Comparator	ilth 3-State Output Pa	~	V	V	16	SDLS008
SN74LS697	20	Synchronous Up/Down Binary Counter	rotalge/F. kiq	~	1 VO	V	er	SDLS199
1002.102	6.010	V V V	Hh 3-State UD Rapieti	N velou	60 manif	116-8	20	ENTER SERVE

commercial package description and availability

PDIP (plastic dual-in-line package)
N = 14/16/20 pins
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NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

 QFP (plastic quad flat package) RC = 52 pins PH = 80 pins

PH = 80 pinsPQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins

PAH = 52 pins PAG = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins **TSSOP** (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



LV Low-Voltage CMOS Technology

TI's LV CMOS technology products are specially designed parts for 3-V power supply use. The entire LV family also has been recharacterized to operate at 5 V.

The LV family is a 2- μ CMOS process that provides up to 8 mA of drive and propagation delays of 18 ns maximum, while having a static power consumption of only 20 μ A for both bus-interface and gate functions.

The LV family is offered in the octal footprints with all of the advanced packaging such as small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), and thin shrink small-outline package (TSSOP).

For LV data sheets, see the 1996 Low-Voltage Logic Data Book, literature number SCBD003B, or the 1996 AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book, literature number SCLD004.

LV

PENIOE	NO.	SISS SOIVED	A	VAILABILI	TY	LITERATURE
DEVICE	PINS	FUNCTION	SOIC	SSOP	TSSOP	REFERENCE
SN74LV00	14	Quad 2-Input Positive-NAND Gate	V	V	~	SCLS182C
SN74LV02	14	Quad 2-Input Positive-NOR Gate	~	~	V	SCLS183B
SN74LV04	14	Hex Inverter	~	V	V	SCLS184C
SN74LVU04	14	Hex Inverter	~	V	V	SCLS185B
SN74LV08	14	Quad 2-Input Positive-AND Gate	~	V	V	SCLS186C
SN74LV14	14	Hex Inverter With Schmitt Trigger	~	V	V	SCLS187B
SN74LV32	14	Quad 2-Input Positive-OR Gate	~	V	V	SCLS188C
SN74LV74	14	Dual D-Type Flip-Flop	~	V	V	SCLS189C
SN74LV125	14	Quad Bus Buffer Gate (OE)	~	V	V	SCES003B
SN74LV138	16	3-to-8 Decoder/Demultiplexer	~	V	V	SCLS190D
SN74LV164	14	8-Bit Parallel-Out Serial Shift Register	~		V	SCLS191B
SN74LV165	16	8-Bit Parallel-Load Shift Register	~	V	V	SCES007B
SN74LV174	16	Hex D-Type Flip-Flop With Clear	~	V	V	SCLS192B
SN74LV240	20	Octal Buffer/Driver	~	V	~	SCLS193B
SN74LV244	20	Octal Buffer/Driver	~	V	V	SCLS194C
SN74LV245	20	Octal Bus Transceiver	~	V	V	SCLS075E
SN74LV273	20	Octal D-Type Flip-Flop With Clear	~	V	V	SCLS195B
SN74LV373	20	Octal D-Type Transparent Latch	~	V	V	SCLS196C
SN74LV374	20	Octal D-Type Flip-Flop	~	~	V	SCLS197B
SN74LV573	20	Octal D-Type Transparent Latch	~	V	V	SCLS198B
SN74LV574	20	Octal D-Type Flip-Flop	V	~	V	SCLS199B

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

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schedule

✓ = Now + = Planned QFP (plastic quad flat package) RC = 52 pins PH = 80 pins

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SOIC (small-outline integrated circuit)
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DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins

PAG = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



LVC Low-Voltage CMOS Technology

TI's LVC logic products are specially designed for 3-V power supplies.

The LVC family is a high-performance version with $0.8-\mu$ CMOS process technology, 24-mA current drive, and 6.5-ns maximum propagation delays for driver operations. The LVC family includes both bus-interface and gate functions with 50 different functions planned.

The LVC family is offered in the octal and Widebus™ footprints with all of the advanced packaging such as small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), and thin shrink small-outline package (TSSOP) with planned thin very small-outline (TVSOP) additions.

All LVC devices are available with 5-V tolerant inputs and outputs.

For LVC data sheets, see the 1996 *Low-Voltage Logic Data Book*, literature number SCBD003B.

LVC

GIND NOUS	NO.	BOIVE		AVAIL	AVAILABILITY		LITERATURE
DEVICE	PINS	FUNCTION	SOIC	SSOP	TSSOP	TVSOP	REFERENCE
SN74LVC00A	14	Quad 2-Input Positive-NAND Gate	V	~	V		SCAS279C
SN74LVC02A	14	Quad 2-Input Positive-NOR Gate	V	V	V		SCAS280C
SN74LVC04A	14	Hex Inverter	~	~	V		SCAS281C
SN74LVCU04A	14	Hex Inverter	V	~	V		SCAS282C
SN74LVC08A	14	Quad 2-Input Positive-AND Gate	V	~	V		SCAS283C
SN74LVC10A	14	Triple 3-Input Positive-NAND Gate	V	~	~		SCAS284C
SN74LVC14A	14	Hex Inverter With Schmitt Trigger	~	~	~		SCAS285C
SN74LVC32A	14	Quad 2-Input Positive-OR Gate	1811	~	V		SCAS286C
SN74LVC74A	14	Dual Positive-Edge-Triggered D-Type Flip-Flop	V	~	V		SCAS287C
SN74LVC86A	14	Quad 2-Input Exclusive-OR Gate	V	V	V		SCAS288C
SN74LVC112A	16	Dual Negative-Edge-Triggered JK Flip-Flop	V	~	V	~	SCAS289C
SN74LVC125A	14	Quad Bus Buffer Gate (OE)	~	~	V		SCAS290C
SN74LVC126A	14	Quad Bus Buffer Gate (OE)	V	V	V	V	SCAS339C
SN74LVC137A	oroo16	3-to-8 Decoder/ Demultiplexer With Address Latches	tern+	+	+		SCAS340B
SN74LVC138A	16	3-to-8 Decoder/ Demultiplexer	avb.	V	V		SCAS291D
SN74LVC139A	16	Dual 2-to-4 Decoder/Demultiplexer	lems+	+	+		SCAS341B
SN74LVC157A	16	Quad 2-to-1 Data Selector/Multiplexer	SETV	~	V		SCAS292C
SN74LVC158A	16	Quad 2-to-1 Data Selector/Multliplexer	+	+	+		SCAS342C
SN74LVC240A	20	Octal Buffer/Driver	/J 18/4	+	+		SCAS293B
SN74LVC241A	20	Octal Buffer/Driver	+	+	+		SCAS343B
SN74LVC244A	20	Octal Buffer/Driver	~	~	V	+	SCAS414D
SN74LVCH244A	20	Octal Buffer/Driver With Bus Hold	~	V	V	+	SCES009A
SN74LVC245A	20	Octal Bus Transceiver	V	V	V	+	SCAS218E
SN74LVCH245A	20	Octal Bus Transceiver With Bus Hold	~	~	V	+	SCES008A
SN74LVC257A	16	Quad 2-to-1 Data Selector/Multliplexer	V	V	V		SCAS294C
SN74LVC258A	16	Quad 2-to-1 Data Selector/Multliplexer	+	+	+		SCAS345C
SN74LVC373A	20	Octal D-Type Transparent Latch	V	V	V		SCAS295D
SN74LVC374A	20	Octal D-Type Flip-Flop	~	V	V		SCAS296D
SN74LVC540A	20	Octal Buffer/Driver	+	+	+		SCAS297C
SN74LVC541A	20	Octal Buffer/Driver	+	+	+		SCAS298C
SN74LVC543A	24	Octal Registered Bus Transceiver	+	+	+	175	SCAS299B

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

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schedule

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D = 8/14/16 pins
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SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package) PAH

= 52 pins = 64 pins PAG PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins



DEVICE	NO.	FUNCTION			ABILITY		LITERATURE
TARBOA HELPHONE	PINS	9088 3108	SOIC	SSOP	TSSOP	TVSOP	REFERENCE
SN74LVC544A	24	Octal Registered Transceiver	gist ed Bu	H (+1)	8+	ASSE	SCAS346B
SN74LVC573A	20	Octal D-Type Transparent Latch	~	V	~	ASB	SCAS300B
SN74LVC574A	20	Octal D-Type Flip-Flop	~	V	V	284	SCAS301A
SN74LVC646A	24	Octal Registered Bus Transceiver	freshtrat	8 + 1	+	A1400	SCAS302B
SN74LVC652A	24	Octal Registered Bus Transceiver	vlapar + iT e	18 (#a)	+	182245A	SCAS303B
SN74LVC821A	24	10-Bit Bus-Interface Flip-Flop	+	+	+		SCAS304B
SN74LVC823A	24	9-Bit Bus-Interface Flip-Flop	+	+	+	+	SCAS305B
SN74LVC827A	24	10-Bit Buffer/ Driver	+	+	+	+	SCAS306C
SN74LVC828A	24	10-Bit Buffer/ Driver	+	+	+	+	SCAS347B
SN74LVC841A	24	10-Bit Bus-Interface D-Type Latch	+	+	+	+	SCAS307C
SN74LVC843A	24	9-Bit Bus-Interface D-Type Latch	+	+	+		SCAS308B
SN74LVC861A	24	10-Bit Bus Transceiver	+	+	+	+	SCAS309B
SN74LVC863A	24	9-Bit Bus Transceiver	+	+	+	+	SCAS310B
SN74LVC2244A	20	Octal Buffer/Driver With Series-Damping Resistors	V	V	V		SCAS572A
SN74LVCR2245	20	Octal Buffer/Driver With Series-Damping Resistors	+	+	+		SCAS581
SN74LVC2952A	24	Octal Registered Bus Transceiver	+	+	+		SCAS311B
SN74LVCC3245	24	Octal Level-Shifting Transceiver	+	+	+		SCAS585
SN74LVC4245	24	Octal Bus Transceiver and 3.3-V to 5-V Shifter	+	+	+		SCAS375B
SN74LVCC4245	24	Octal Level-Shifting Transceiver	+	+	+	15	SCAS584
SN74LVCH16240A	48	16-Bit Buffer/Driver With Bus Hold		V	V	+	SCAS566B
SN74LVCH16241A	48	16-Bit Buffer/Driver With Bus Hold		+	+		SCAS348B
SN74LVC16244A	48	16-Bit Buffer/Driver		V	V	+	SCES061B
SN74LVCH16244A	48	16-Bit Buffer/Driver With Bus Hold		V	V		SCAS313C
SN74LVC16245A	48	16-Bit Bus Transceiver	and Heli	V	V	+	SCES062B
SN74LVCH16245A	48	16-Bit Bus Transceiver With Bus Hold		V	V	V	SCES063B
SN74LVCH16373A	48	16-Bit Transparent D-Type Latch With Bus Hold		V	V	+	SCAS568B
SN74LVCH16374A	48	16-Bit Edge-Triggered D-Type Flip-Flop With Bus Hold		V	V	+	SCAS565B
SN74LVCH16540A	48	16-Bit Buffer/ Driver With Bus Hold		~	V	+	SCAS569B
SN74LVCH16541A	48	16-Bit Buffer/ Driver With Bus Hold		V	V	+	SCAS567B
SN74LVCH16543A	56	16-Bit Registered Bus Transceiver With Bus Hold		+	+	+	SCAS317B
SN74LVCH16646A	56	16-Bit Registered Bus Transceiver With Bus Hold		+	+	+	SCAS318C

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D = 8/14/16 pins DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

PAH = 52 pins = 64 pins PAG PM = 64 pins PN = 80 pins PCA, PZ = 100 pins = 120 pins PCB

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins



LVC

DEVICE	10897	NO. PINS			FUNCTION		SOIC	AVAILA	ABILITY	TVSOP	LITERATURE
SN74LVCH166	652A	56	16-Bit Re	egistered Bu	us Transceiver With	Bus Hold	anii berafelos	8 (+)0	1+	+ A	SCAS319C
SN74LVC1695	52A	56	16-Bit Re	egistered Bu	us Transceiver	ront Latch	Тура Тгалара	01+00	0+	+ /	SCAS320B
SN74LVC1612	284	48	17-Bit IE	EE P1284 [Driver/Receiver	9	Type Plip-Flo	0.400	0+	+ A	SCAS583
SN74LVCH162	2244A	48	16-Bit Bu	Iffer/Driver	With Series-Dampir	ng Resistors and Bo	us Hold	R 1+00	+	+ 6	SCAS545A
SN74LVCHR1	62245A	48	16-Bit Bu	s Transceiv	ver With Series-Dar	nping Resistors and	d Bus Hold	R 14:00	+	A	SCAS582
SCASSONE		+	+	+		qoPl-qir	e Interface P	10-88 8	24	A	SNZ4LVC821
									24		
											SNT/ALVG208

commercial package description and availability

PDIP (plastic dual-in-line package)

N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins

PQ = 100/132 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins PAH PAG PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



LVT Low-Voltage BiCMOS Technology

The specially designed 3-V LVT family uses the latest 0.8- μ BiCMOS-process technology for bus-interface functions. Like its 5-V ABT counterpart, LVT can provide up to 64 mA of drive, 4-ns propagation delays, and in addition, consumes less than 100 μ A of standby power. The inputs have the bus-hold feature to eliminate external pullup resistors and I/Os that can handle up to 7 V, which allows them to act as 5-V/3-V translators.

LVTZ devices offer all the features found in TI's standard LVT family. In addition, LVTZ incorporates circuitry to protect the devices in live-insertion applications. The device goes to the high-impedance state during power up and power down, which is called powered-up 3 state (PU3S).

The LVT family is offered in the octal and Widebus™ footprints with all of the advanced packaging such as small-outline integrated circuit (SOIC), shrink small-outline package (SSOP), and thin shrink small-outline package (TSSOP).

For LVT data sheets, see the 1996 *Low-Voltage Logic Data Book*, literature number SCBD003B.

LVT

DEVICE	NO.	FUNCTION			AVAILABI	LITY		LITERATURE
DEVICE	PINS	TONOTION	MIL	SOIC	SSOP	TSSOP	TVSOP	REFERENCE
SN74LVT125	14	Quad Bus Buffer Gate (OE)		~	~	V		SCBS133D
SN74LVT240	20	Octal Buffer/Driver		~	V	~		SCBS134G
SN74LVT241	20	Octal Buffer/Driver		V	V	~		SCBS352
SN74LVT244A	20	Octal Buffer/Driver	V	~	V	~		SCAS354C
SN74LVTH245A	20	Octal Bus Transceiver	~	V	~	~		SCBS130K
SN74LVTR2245	20	Octal Bus Transceiver	NO.	+	+	+		Call
SN74LVT273	20	Octal D-Type Flip-Flop With Clear		~	V	~		SCBS136F
SN74LVTH540	20	Octal Buffer/Driver	eds et	T+	+	+		Call
SN74LVTH541	20	Octal Buffer/Driver	plonribe	et +	+	+		Call
SN74LVT543	24	Octal Registered Bus Transceiver	ebivor	1	~	V		SCBS137D
SN74LVT573	20	Octal D-Type Transparent Latch	~	V	V	~		SCBS138D
SN74LVT574	20	Octal D-Type Flip-Flop	V	V	~	V		SCBS139D
SN74LVT646	24	Octal Registered Bus Transceiver	V	V	V	V		SCBS140D
SN74LVT652	24	Octal Registered Bus Transceiver			V	V		SCBS141E
SN74LVT2952	24	Octal Registered Bus Transceiver	malili-t	V	V	V		SCBS152E
SN74LVTH16244A	48	16-Bit Buffer/Driver	taniina		V	V		SCBS142H
SN74LVTH16245A	48	16-Bit Bus Transceiver	una ba		V	V		SCBS143G
SN74LVTH16373	48	16-Bit D-Type Transparent Latch			V	V		SCBS144G
SN74LVTH16374	48	16-Bit D-Type Flip-Flop	TVJ en	T	V	V		SCBS145G
SN74LVT16500	56	18-Bit Universal Bus Transceiver	dyano	8	~	V	3576	SCBS146D
SN74LVT16501	56	18-Bit Universal Bus Transceiver	io-llam	13	V	V		SCBS147G
SN74LVT16543	56	16-Bit Registered Transceiver	10881)	V	V		SCBS148C
SN74LVT16646	56	16-Bit Registered Bus Transceiver			V	V		SCBS149C
SN74LVT16835	56	18-Bit Buffer/Driver	TVJ 10	4	V	~		SCBS309D
SN74LVT16952	56	16-Bit Registered Bus Transceiver	V	n	V	~		SCBS151D
SN74LVT162244	48	16-Bit Buffer/Driver With Series Resistors	V		~	V		SCBS258F
SN74LVTH162244	48	16-Bit Buffer/Driver With Series Resistors			V	V		SCBS258F
SN74LVT162245	48	16-Bit Bus Transceiver With Series Resistors		13-41	V	V		SCBS260E
SN74LVTH162245	48	16-Bit Bus Transceiver With Series Resistors	+		V	V		Call
SN74LVTH162373	48	16-Bit D-Type Transparent Latch With Series Resistors			~	V		SCBS261E
SN74LVTH162374	48	16-Bit D-Type Flip-Flop With Series Resistors			V	V	West.	SCBS262D

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule ✓ = Now + = Planned QFP (plastic quad flat package) RC = 52 pins PH = 80 pins

PQ = 100/132 pinsSOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins

PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



LVT

DEVICE	NO.	FUNCTION	FUNCTION		AVAILABILITY				
	PINS	FUNCTION			SSOP	TSSOP	TVSOP	REFERENCE	
SN74LVTZ240	20	Octal Buffer/Driver		V	V	~		SCBS301B	
SN74LVTZ244	20	Octal Buffer/Driver		~	V	V		SCBS302C	
SN74LVTZ245	20	Octal Bus Transceiver		V	V	V		SCBS303C	

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

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DB = 14/16/20/24/28/30/38 pins
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SOT (small-outline transistor)

DBV = 5 pins

TQFP (plastic thin quad flat package)

= 52 pins = 64 pins PAH PAG PM = 64 pins

PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package) PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



TVU

	N	V		

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PDIP (nissto duskio-line packtige) R = 14/15/20 pins

N = 14/19/20 pics NT = 24/26 pics

PLQG (physic jungus only control PH = 20128/44/52/08/64 phys

phubodos - No.

POT (mesh-ciptine translation)

10 V = 5 pins

10 V

TOPP (plants the quad flor PAR = 62 plas RAG = 54 plas

794 = 6- prins POA, PZ = 100 pins POB = 120 pins

TSBOP (nin shrink amal-publike parksige)
PW - SHAFR (SCREAKS pins
DGG - 48/25/04 pins

TVSOP (min very sitelli cutina p DCN = 14/18/00/24/46/65 pins

Mil. - relev to page 4-1 for military padange disemptons and availability

S Schottky Logic

While the overall demand for S products is declining, there remains significant interest in the marketplace for many of these functions. TI will continue to supply S products as long as there is an appropriate level of market demand for them.

The S family is not recommended for new designs.

For S data sheets, contact the Product Information Center at (972) 644-5580.

BENJAT	NO.	RIBS BOIVEO		LITERATURE		
DEVICE	PINS	FUNCTION	MIL	PDIP	SOIC	REFERENCE
SN74S00	14	Quad 2-Input Positive-NAND Gate	~	V	V	SDLS025
SN74S02	14	Quad 2-Input Positive-NOR Gate	~	V	V	SDLS027
SN74S04	14	Hex Inverter	V	V	V	SDLS029
SN74S05	14	Hex Inverter With Open-Collector Outputs	~	V	V	SDLS030
SN74S08	14	Quad 2-Input Positive-AND Gate	~	V	V	SDLS033
SN74S09	14	Quad 2-Input Positive-AND Gate With Open-Collector Outputs	~	V	V	SDLS034
SN74S10	14	Triple 3-Input Positive-NAND Gate	V	V	V	SDLS035
SN74S11	14	Triple 3-Input Positive-AND Gate	V	V	V	SDLS131
SN74S20	14	Dual 4-Input Positive-NAND Gate	~	V	V	SDLS079
SN74S30	14	8-Input Positive-NAND Gate	~	V	V	SDLS099
SN74S32	14	Quad 2-Input Positive-OR Gate	V	V	V	SDLS100
SN74S37	14	Quad 2-Input Positive-NAND Gate	V	V	V	SDLS103
SN74S38	14	Quad 2-Input NAND Gate With Open-Collector Outputs	V	V	V	SDLS105
SN74S51	14	Dual 2-Input and Dual 3-Input AND/OR Gate	V	V	V	SDLS113
SN74S74	14	Dual D-Type Flip-Flop	V	V	V	SDLS119
SN74S85	14	4-Bit Magnitude Comparator	V	V	V	SDLS123
SN74S112A	16	Dual J-K Negative-Edge-Triggered Flip-Flop	V	V	V	SDLS011
SN74S124	16	Dual Voltage-Controlled Oscillator	~	V	V	SDLS201
SN74S132	14	Quad 2-Input Positive-NAND Schmitt Trigger	V	V	V	SDLS047
SN74S133	16	13-Input NAND Gate	V	V	V	SDLS202
SN74S138A	16	3-to-8 Decoder/Demultiplexer	V	V	V	SDLS014
SN74S139A	16	Dual 2-to-4 Decoder/Demultiplexer	V	V	V	SDLS013
SN74S140	14	Dual 50-Ω Line Driver	V	V	V	SDLS210
SN74S151	16	8-to-1 Data Selector/Multiplexer	V	~	~	SDLS054
SN74S153	16	Dual 4-to-1 Data Selector/Multiplexer	V	V	V	SDLS055
SN74S157	16	Quad 1-of-2 Data Selector/Multiplexer	V	V	V	SDLS058
SN74S158	16	Quad 2-to-1 Data Selector/Multiplexer	~	V	V	SDLS058
SN74S163	16	4-Bit Synchronous Binary Counter	V	V	V	SDLS060
SN74S169	16	4-Bit Synchronous Up/Down Binary Counter	~	V		SDLS134
SN74S174	16	Hex D-Type Flip-Flop	V	V		SDLS068
SN74S175	16	Quad D-Type Flip-Flop	V	V	V	SDLS068

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule ✓ = Now + = Planned

QFP (plastic quad flat package) RC = 52 pins PH = 80 pins

PQ = 100/132 pins SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package) = 52 pins = 64 pins PAG = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



DEVICE	NO.	FUNCTION	A	AVAILABILITY			
DEVICE	PINS	FONCTION	MIL	PDIP	SOIC	REFERENCE	
SN74S194	16	4-Bit Bidirectional Universal Shift Register	V	V		SDLS075	
SN74S195	16	4-Bit Bidirectional Universal Shift Register	~	V	~	SDLS076	
SN74S240	20	Octal Buffer/Driver	V	V	~	SDLS144	
SN74S241	20	Octal Buffer/Driver	V	V	V	SDLS144	
SN74S244	20	Octal Buffer/Driver	~	V	~	SDLS144	
SN74S251	16	1-of-8 Data Selector/Multiplexer	· ·	V	~	SDLS085	
SN74S257	16	Quad 2-to-1 Data Selector/Multiplexer	~	V	~	SDLS148	
SN74S260	14	Dual 5-Input Positive-NOR Gate	~	V	~	SDLS208	
SN74S280	14	9-Bit Parity Generator/Checker	V	V	V	SDLS152	
SN74S283	16	4-Bit Binary Full Adder	~	V		SDLS095	
SN74S299	20	8-Bit Universal Shift Register	~	V	~	SDLS156	
SN74S373	20	Octal D-Type Transparent Latch	V	V	V	SDLS165	
SN74S374	20	Octal D-Type Flip-Flop	V	~	V	SDLS165	
SN74S381	20	Arithmetic Logic Unit	V	V		SDLS168	

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins

PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

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= Now + = Planned QFP (plastic quad flat package)

RC = 52 pins PH = 80 pins PQ = 100/132 pins

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SOIC (small-outline integrated circuit)
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TVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins



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PLOT (photo leaded only center Fil. - 2022/44/2010/64 pins

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 P plastic quedifit partiage)
 SDT (armin outline transport

 = 30 pms
 36V = 6 pms

 = 50 pms
 TGPP (disable this quedifit)

 = 100 ms
 TGPP (disable this quedifit)

TURP (please trans PM) = 62 pms RN3 = 64 pms

P\$\$ = \$4 pinn
P\$ -- \$6 pinn
P\$A, P\$ -- \$10 pin
P\$B -- \$10 pin

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TTL Transistor-Transistor Logic

While the overall demand for TTL products is declining, there remains significant interest in the marketplace for many of these functions. TI will continue to supply TTL products as long as there is an appropriate level of market demand for them.

With the exception of the SN7406 and SN7407, the TTL family is not recommended for new designs.

For TTL data sheets, contact the Product Information Center at (972) 644-5580.

TTL

DEVICE	NO.	FUNCTION	AVAILABILITY			LITERATURE
DEVICE	PINS	FONCTION	MIL	PDIP	SOIC	REFERENCI
SN7400	14	Quad 2-Input Positive-NAND Gate	V	V	V	SDLS025
SN7404	14	Hex Inverter	V	~		SDLS029
SN7405	14	Hex Inverter With Open-Collector Outputs	~	V	~	SDLS030
SN7406	14	Hex Inverter With Open-Collector Outputs	V	V	~	SDLS031
SN7407	14	Hex Buffer With Open-Collector Outputs	~	V	~	SDLS032
SN7414	14	Hex Inverter With Schmitt Trigger	V	~	V	SDLS049
SN7416	14	Hex Inverter/Driver	V	V	V	SDLS031
SN7417	14	Hex Buffer/Driver With Open-Collector Outputs	V	V	V	SDLS032
SN7430	14	8-Input Positive-NAND Gate	V	V		SDLS099
SN7432	14	Quad 2-Input OR Gate	V	V		SDLS100
SN7437	14	Quad 2-Input Positive-NAND Gate	V	V		SDLS103
SN7438	14	Quad 2-Input Positive-NAND Gate With Open-Collector Outputs	V	V	V	SDLS105
SN7445	16	BCD-to-Decimal Decoder/Driver	V	V		SDLS110
SN7447A	16	BCD 7-Segment Decoder/Driver	V	V		SDLS111
SN7474	14	Dual D-Type Flip-Flop	V	V	V	SDLS119
SN7497	16	Binary Rate Multiplier	V	V		SDLS130
SN74121	14	One-Shot Multivibrator	V	V	V	SDLS042
SN74123	16	Dual Monostable Multivibrator	V	V		SDLS043
SN74128	14	50-Ω Line Driver	V	V	V	SDLS045
SN74132	14	Quad 2-Input Positive-NAND With Schmitt Trigger	V	V		SDLS047
SN74145	16	BCD-to-Decimal Decoder/Driver	V	V		SDLS051
SN74148	16	8-to-3-Line Priority Encoder	~	V		SDLS053
SN74150	24	Data Selector/Multiplexer	V	V		SDLS054
SN74154	24	4-to-16-Line Decoder/Demultiplexer	V	V	V	SDLS056
SN74156	16	Dual 2-to-4-Line Decoder/Demultiplexer With Open-Collector Outputs	V	V		SDLS057
SN74157	16	Quad 2-to-1 Data Selector/Multiplexer	V	V	Hai	SDLS058
SN74159	24	4-to-16-Line Decoder/Demultiplexer	V	V		SDLS059
SN74175	16	Quad D-Type Flip-Flop	V	V		SDLS068
SN74193	16	4-Bit Synchronous Up/Down Binary Counter	V	V		SDLS074
SN74276	20	Quad J-K Flip-Flop		V	V	SDLS091
SN74367A	16	Hex Buffer/Driver	V	V		SDLS102

commercial package description and availability

PDIP (plastic dual-in-line package) N = 14/16/20 pins NT = 24/28 pins NP = 28 pins PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins

schedule

✓ = Now + = Planned

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DW = 16/20/24/28 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins

SOT (small-outline transistor) DBV = 5 pins

TQFP (plastic thin quad flat package) PAH = 52 pins = 64 pins PAG PAG = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80/100 pins



TTL

DEVICE	NO. PINS		FUNCTION	A	LITERATURE		
			FUNCTION	MIL	PDIP	SOIC	REFERENCE
SN74368A	16	Hex Buffer/Driver		V	V		SDLS102
SN74376	16	Quad J-K Flip-Flop		V	V		SDLS104

commercial package description and availability

PDIP (plastic dual-in-line package) TSSOP (thin shrink small-outline package) QFP (plastic quad flat package) SOT (small-outline transistor) N = 14/16/20 pins NT = 24/28 pins RC = 52 pins PH = 80 pins PW = 8/14/16/20/24/28 pins DGG = 48/56/64 pins DBV = 5 pins TQFP (plastic thin quad flat package) NP = 28 pins PQ = 100/132 pinsTVSOP (thin very small-outline package) DGV = 14/16/20/24/48/56 pins DBB = 80/100 pins = 52 pins = 64 pins PAH PLCC (plastic leaded chip carrier) FN = 20/28/44/52/68/84 pins SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins PAG PAG = 64 pins PM = 64 pins PN = 80 pins PCA, PZ = 100 pins PCB = 120 pins schedule **SSOP** (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DL = 28/48/56 pins ✓ = Now MIL – refer to page 4–1 for military package description and availability + = Planned



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